OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE

Superconducting Computing and the IARPA C3 Program

LEADING INTELLIGENCE INTEGRATION

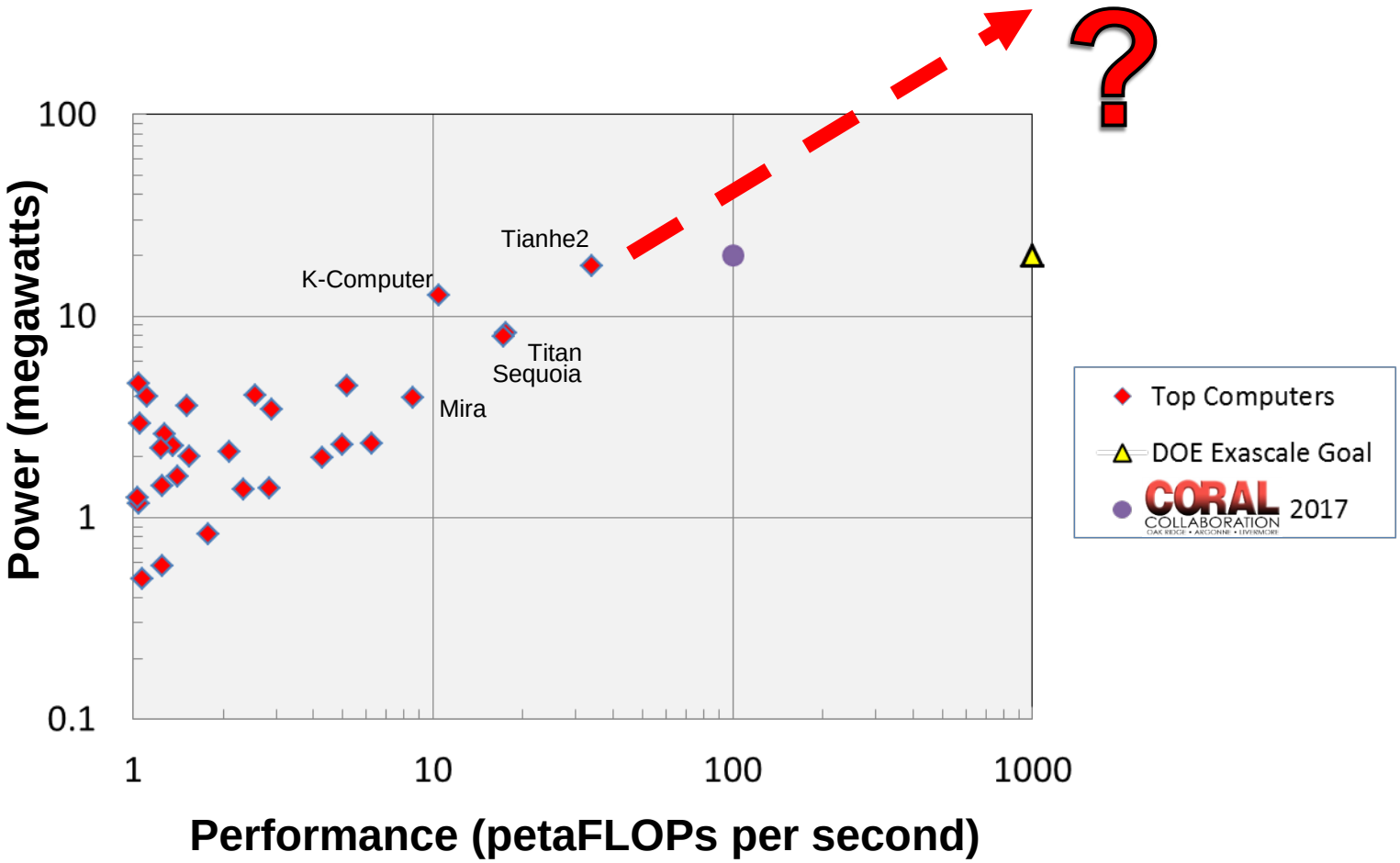
Dr. D. Scott Holmes, Booz Allen Hamilton
IARPA C3 Program Technical Support

Beyond CMOS Workshop, 2016 April 4-5

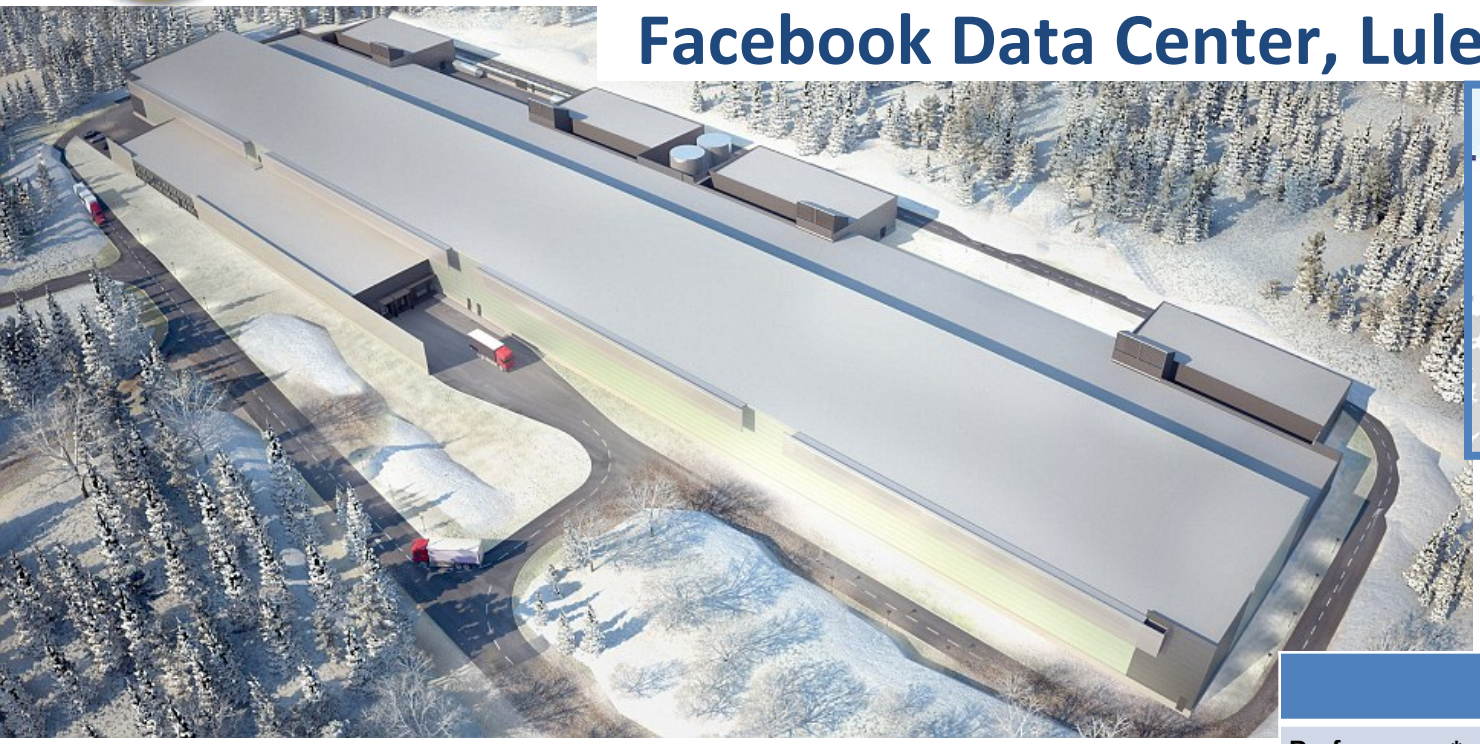
Superconducting Computing and the IARPA C3 Program

- Problems in large scale computing
- Feasibility study
- Cryogenic Computing Complexity (C3) program (IARPA)
- Challenges
- Related work
- Conclusions

Problem: Increasing power requirements for conventional supercomputers



Facebook Data Center, Luleå, Sweden



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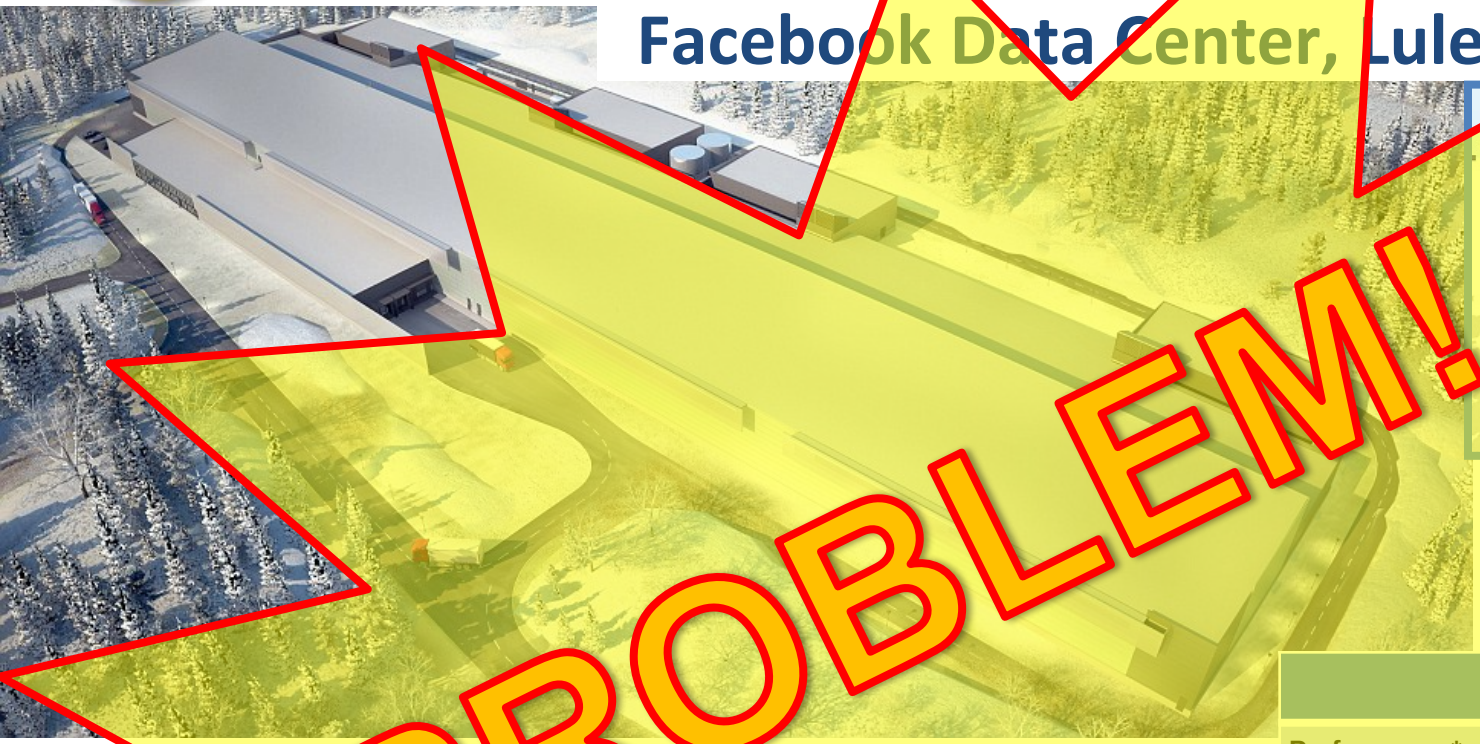
Facebook

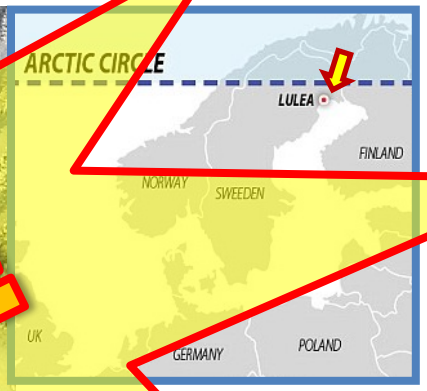
- 2014 completion target
- Cost: ~760 M$
- Nearby Lule River generates
  9% of Sweden's electricity (~4.23 GW)
- Average annual temperature: 1.3 °C

	Specifications
Performance*	**27-51 PFLOP/s**
Memory*	**21-27** PB RAM **1900-6800** PB disk
Power	**84** MW avg* (120 MW max)
Space	**290,000** ft^2 (27,000 m^2)
Cooling*	~1.07 PUE

* estimated

Facebook Data Center, Luleå, Sweden





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PROBLEM!

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The Problem is Power-Space-Cooling

- Upgrading a facility to more powerful computers is constrained by
  - ***Power*** supply capability of electric company
  - ***Space*** limitations
  - ***Cooling*** infrastructure

- Constraints on developing computers with additional processing power
  - Some estimates to reach exascale are in the hundreds of megawatts.
  - An exascale computer at 20 megawatts based on semiconducting technology will require heroic measures.
  - We will require a different technology to get beyond exascale.

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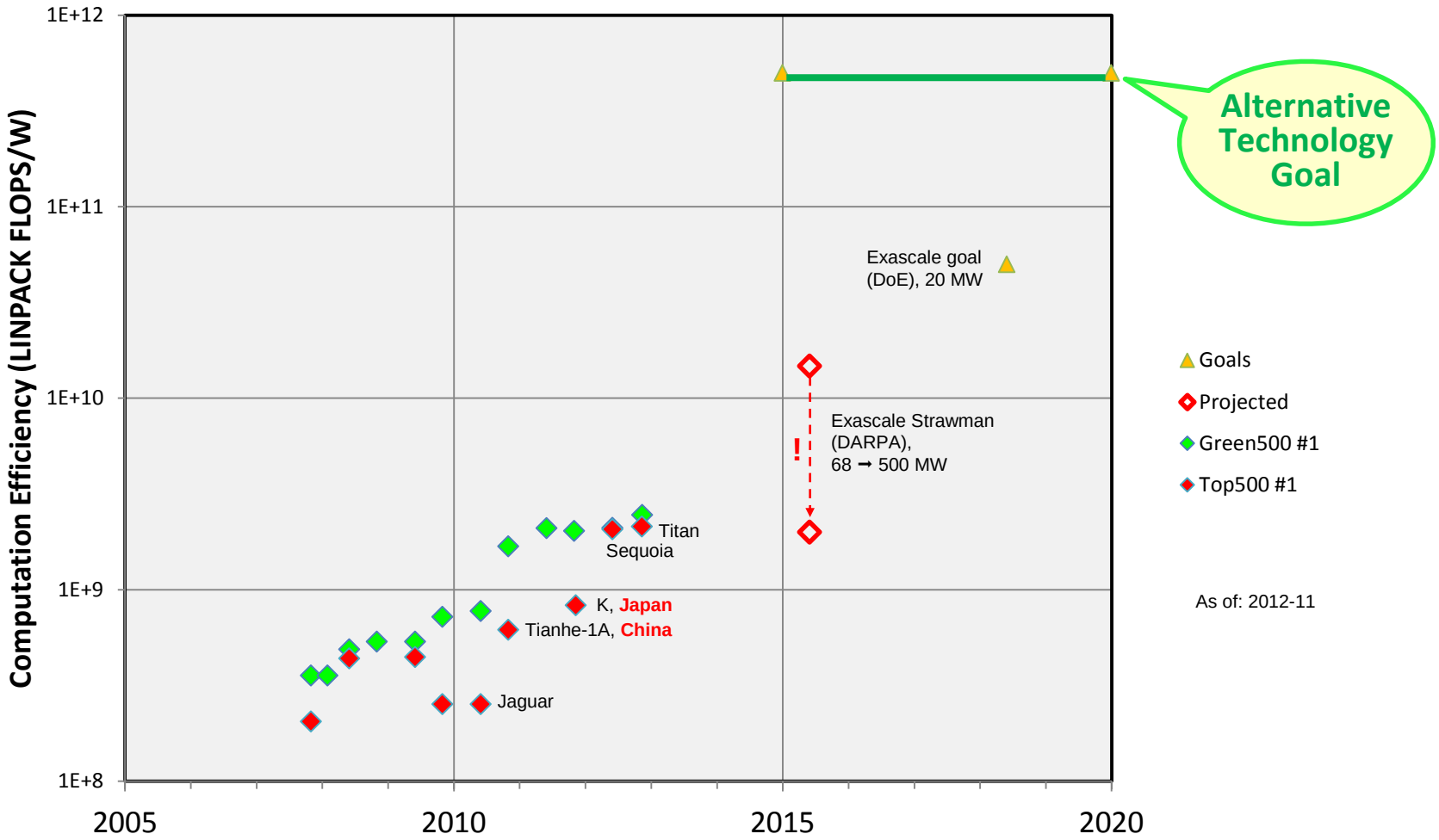
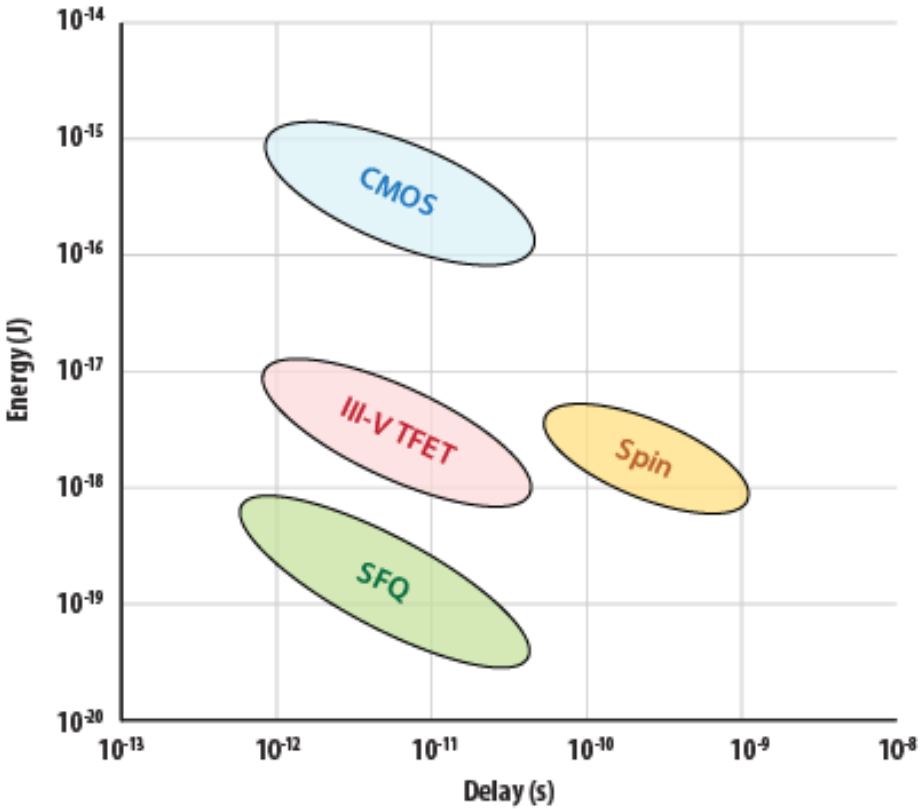
Goal: Computation Efficiency



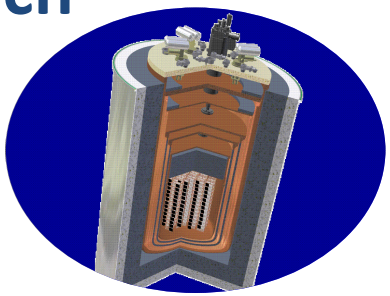
Alternative Technologies



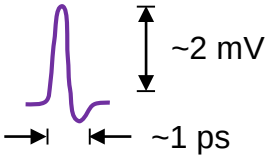
MIT Lincoln Laboratory, "Forecasting superconductive electronics technology," The Next Wave, vol. 20, no. 3, 2014.
https://www.nsa.gov/research/tnw/tnw203/article2.shtml

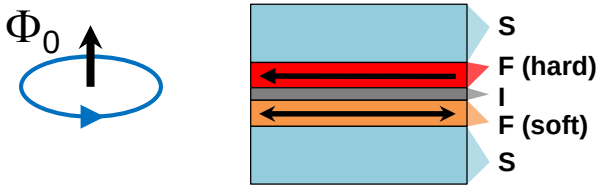
- Superconducting SFQ (single flux quantum) looks good based on switching energy-delay, **but**:
  - Refrigeration requires x400 to x5000 energy
  - Wiring + leakage losses dominate for other technologies
- Conclusions:
  - Full system evaluation is required for SFQ
  - Better metrics and figures-of-merit needed!

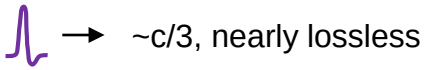
Superconducting Computing Approach



- Low temperature operation (~4 K)
  - Allows different physics
  - Commercially available refrigeration
- **Logic**
  - SFQ (Single Flux Quantum)
  - Switching energy ~ 2×10^{-20} J
- **Memory**
  - compatible with SFQ logic
- **Interconnects**
  - Superconducting in the cold space
  - Input/Output: electrical or optical
- Major energy reductions in all 3 areas!

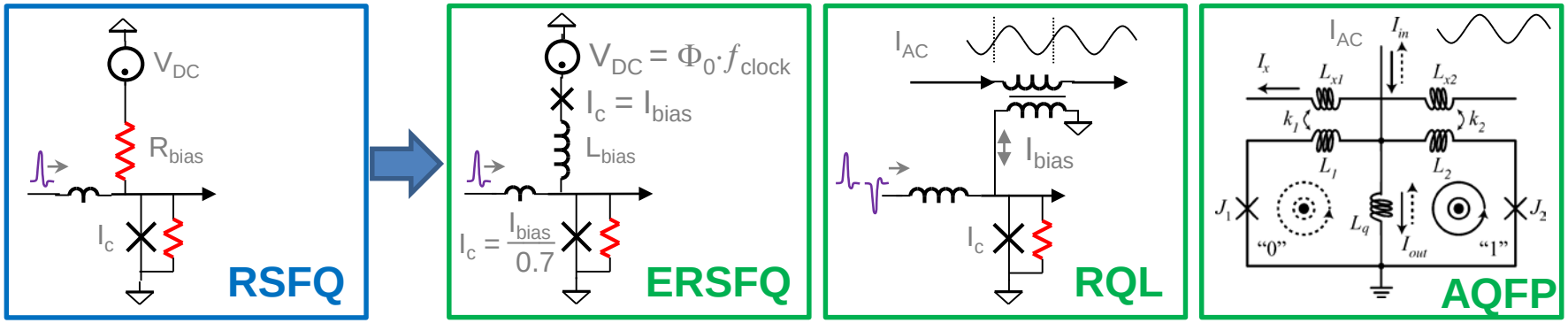






Feasibility Study

- Superconducting supercomputer evaluation using:
  - ***Near-zero energy*** 4 K interconnect
  - ***New*** SFQ logic with no static power dissipation
  - ***New*** cryogenic memory ideas
  - ***Electrical*** *or* ***optical*** input and output
  - ***Commercial*** cryogenic refrigerators



Rapid Single Flux Quantum

Energy-efficient Rapid Single Flux Quantum (Hypres)

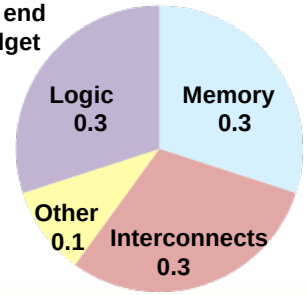
Reciprocal Quantum Logic (NGC)

Adiabatic Quantum Flux Parametron

System Power Budgets

Performance (PFLOP/s):	1	10	100	1,000
(qty) Refrigeration system, LHe recondensing (cost) • Heat load at cold end * • Cooling penalty (300 K/4 K)	(1) SHI model SRDK-415D-F50 (45 k$) • 1.5 W @ 4.2 K • 5000 W/W	(2) SHI GM-JT CG310SLCR (320 k$) • 10 W @ 4.3 K • 1280 W/W	(1) Linde LR70 helium liquefier (2 M$) • 100 W @ 4.4 K • 450 W/W	(2) Linde LR280 helium liquefier (6 M$) • 1,020 W @ 4.4 K • 395 W/W
Power – cooling (60 Hz)	**7.5** kW	**12.8** kW	**45** kW	**400** kW
Power – everything else	**7.5** kW	**27.2** kW	**155** kW	**1,600** kW
Total system power	**15** kW	**40** kW	**200** kW	**2,000** kW
• Computation efficiency (goal: $\geq 5 \times 10^{11}$ FLOPS/W)	0.7×10^{11} FLOPS/W	2.5×10^{11} FLOPS/W	5×10^{11} FLOPS/W	5×10^{11} FLOPS/W

* typical cold end heat load budget



- Toughest problem: scaling uncooled components, primarily disk storage memory

Memory Power @ 4 K

- Cryogenic operation preferred: close to logic, so low latency
  - Superconducting interconnects for speed, low energy loss

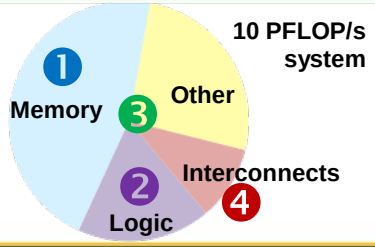
Performance (PFLOP/s)	1	10	100	1,000
Main memory (1 B·s/FLOP)	1 PB	10 PB	100 PB	1,000 PB
Power budget (@ 4 K) • target for memory	1.5 W 0.4 W	10 W 3 W	100 W 30 W	1,000 W 300 W
Hybrid JJ-CMOS (Van Duzer 2007), 20 mW/MiB	19 MW	190 MW	1.9 GW	19 GW
Pipelined dc SFQ RAM (SRL 2005), 700 µW/8 KiB (100 µV power supply)	86 MW	860 MW	8.6 GW	86 GW
Josephson MRAM (NG proposal) 1 B/FLOP, R/W: 5/160 aJ/bit	0.46 W	4.6 W	46 W	460 W

ASC 2012 paper 3EA-03, "Josephson MRAM", A. Herr et al.

JMRAM approach might work

System feasibility study: power @ 4 K

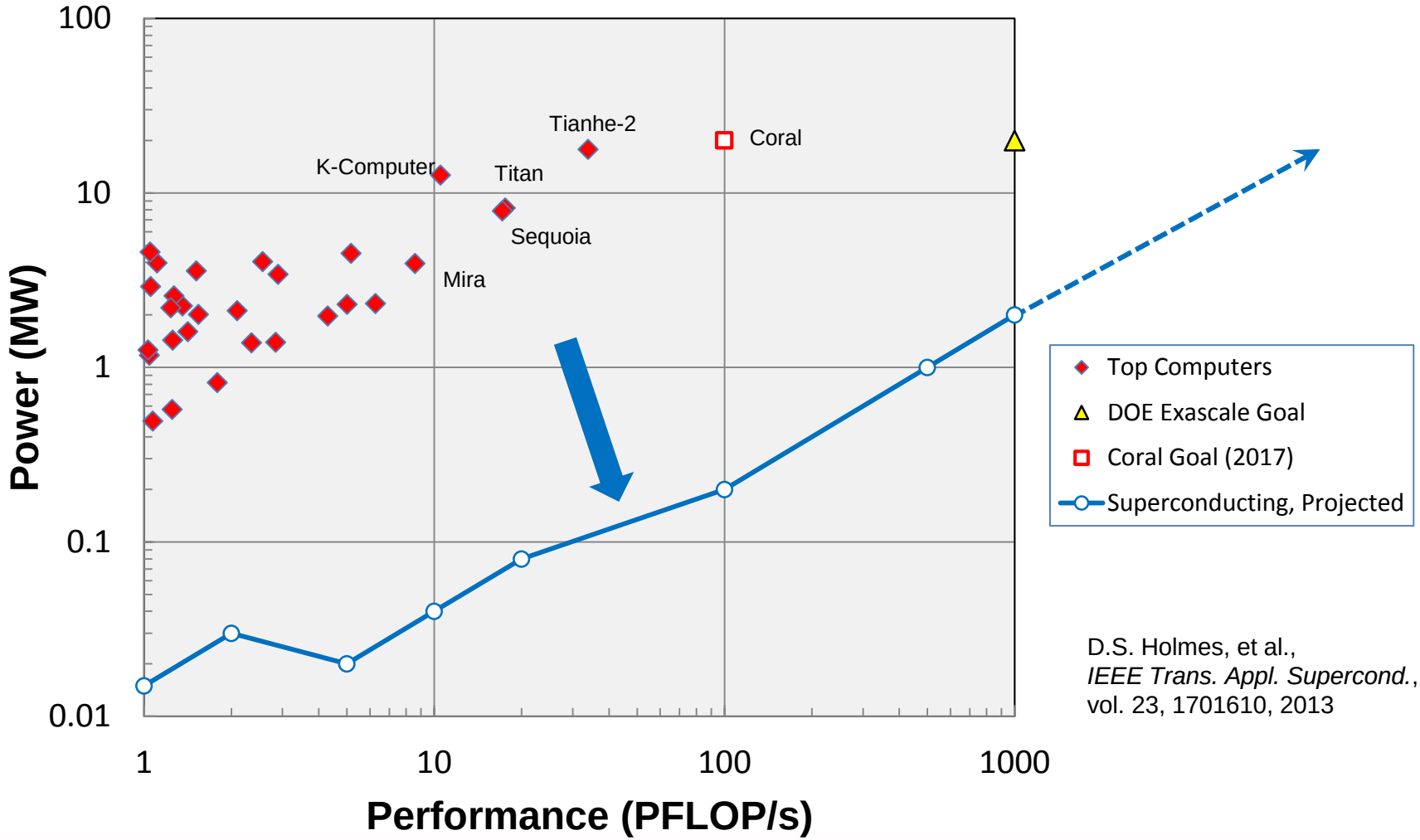
Performance (PFLOP/s):	1	10	100	1,000
Power budget (@ 4 K)	1.5 W	10 W	100 W	1,000 W
Logic (RQL, Ic = 25 µA, 8.3 GHz) • processor cores	**0.18** W • 40,200	**1.8** W • 402,000	**18** W • 4,020,000	**180** W • 40,200,000
Memory (1 B/FLOP, JMRAM) • quantity (1 B/FLOPS)	**0.46** W 1 PB	**4.6** W 10 PB	**46** W 100 PB	**460** W 1,000 PB
Interconnects (VCSELs @ 40 K)	**0.1** W	**1** W	**10** W	**100** W
Other (structure, radiation heat leaks)	**0.76** W	**2.6** W	**26** W	**260** W
Total	**1.5** W	**10** W	**100** W	**1,000** W
• Computation efficiency (goal: ≥ 5 x 10^{11} FLOPS/W)	0.7 x 10^{11} FLOPS/W	2.5 x 10^{11} FLOPS/W	**5 x 10^{11}** FLOPS/W	**5 x 10^{11}** FLOPS/W



Conclusions:

- Energy-efficient superconducting computers are possible
- Priorities: **Memory** → **Logic** → **System** → **Interconnects**

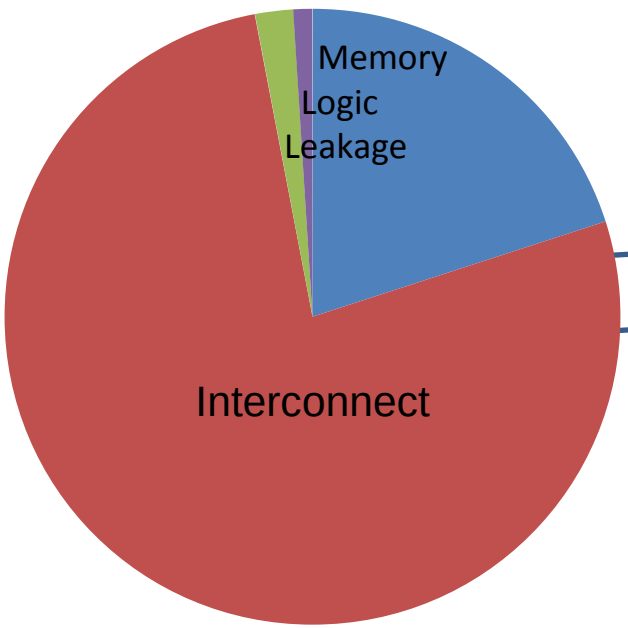
Superconducting computing looks promising



D.S. Holmes, et al., *IEEE Trans. Appl. Supercond.*, vol. 23, 1701610, 2013

Exascale Power Comparison

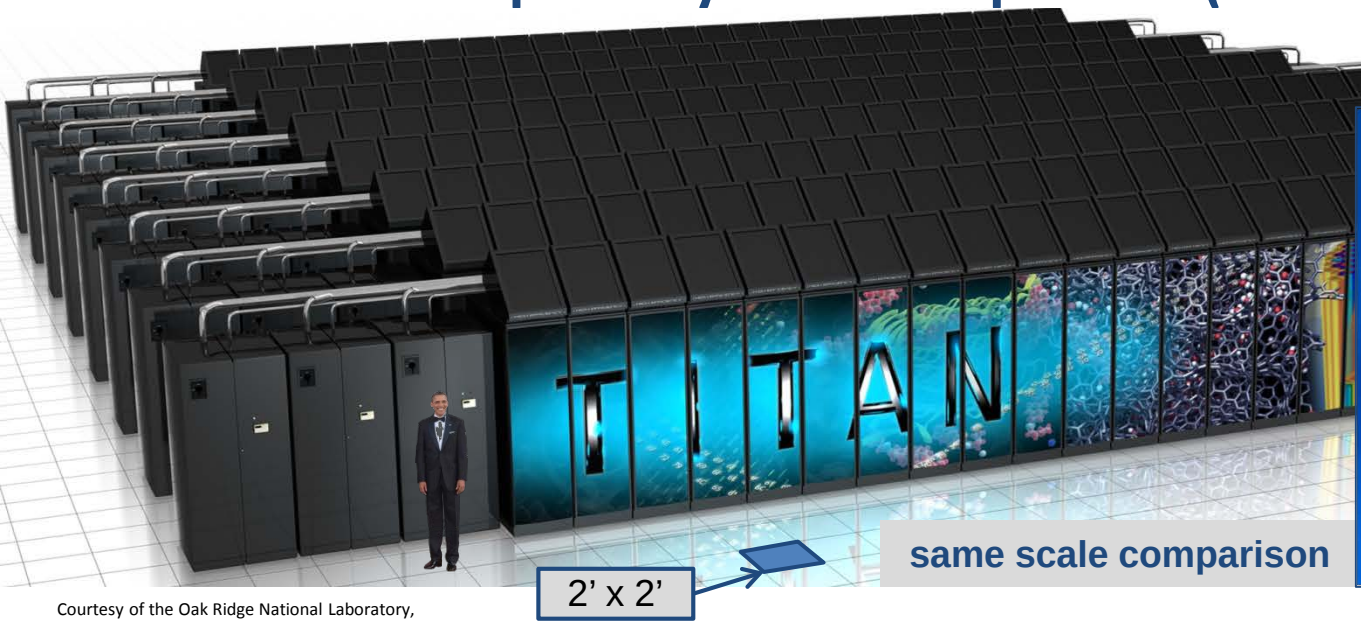
Conventional computer at 100 MW



Superconducting computer at 2 MW

Biggest win is superconducting interconnect!

Conceptual System Comparison (~20 PFLOP/s)



Courtesy of the Oak Ridge National Laboratory, U.S. Department of Energy

same scale comparison

Courtesy of IARPA

	Titan at ORNL	Superconducting Supercomputer	
Performance	**17.6** PFLOP/s (#2 in world*)	**20** PFLOP/s	~1x
Memory	**710** TB (0.04 B/FLOPS)	**5** PB (0.25 B/FLOPS)	7x
Power	**8,200** kW avg. (not included: cooling, storage memory)	**80** kW total power (includes cooling)	0.01x
Space	**4,350** ft^2 (404 m^2, not including cooling)	~**200** ft^2 (19 m^2, includes cooling)	0.05x
Cooling	additional power, space and infrastructure required	All cooling shown	

* TOP500, 2015-11

Superconducting Computing and the IARPA C3 Program

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- Challenges
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Cryogenic Computing Complexity (C3) program goal

Develop technologies for a computer based on superconducting logic with cryogenic memory, and

Integrate a prototype that can answer these questions:

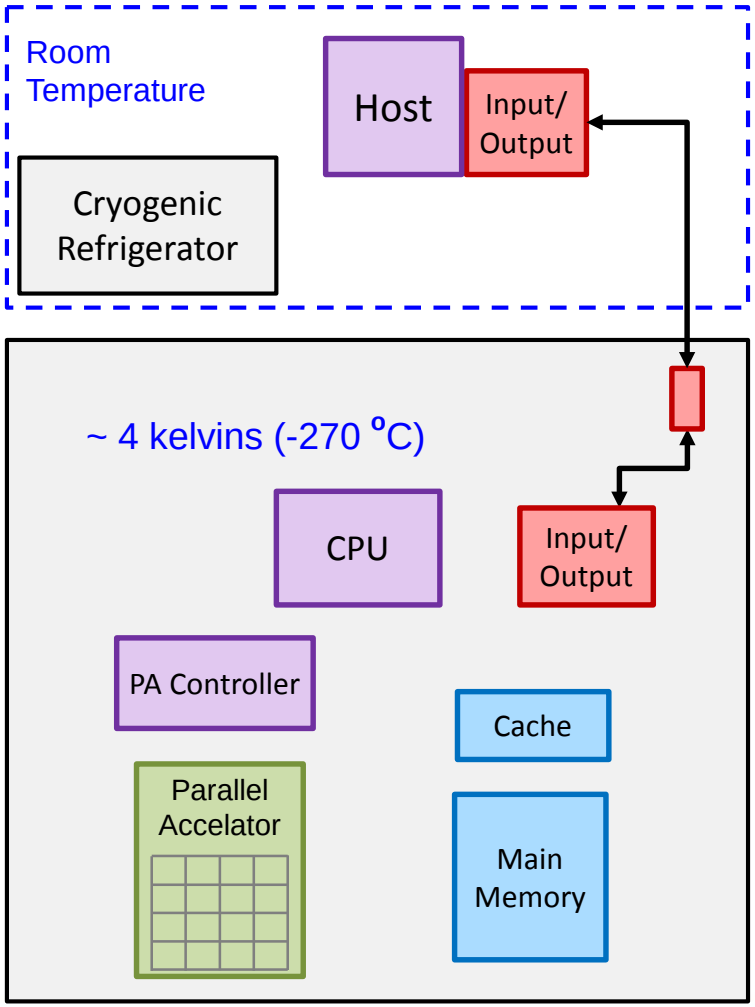
1) Can we build a superconducting computer that is capable of solving important problems?
2) Does it provide a sufficient advantage over conventional computing that we want to build it?

C3 development areas

- Approach based on:
  - *Near-zero energy* superconducting **interconnect**
  - *New* SFQ **logic** with no static power dissipation
  - *New energy efficient* cryogenic **memory** ideas
  - ***Electrical or optical*** inputs and outputs
  - ***Commercial*** cryogenic refrigerators

IARPA C3 program basis

Notional Prototype



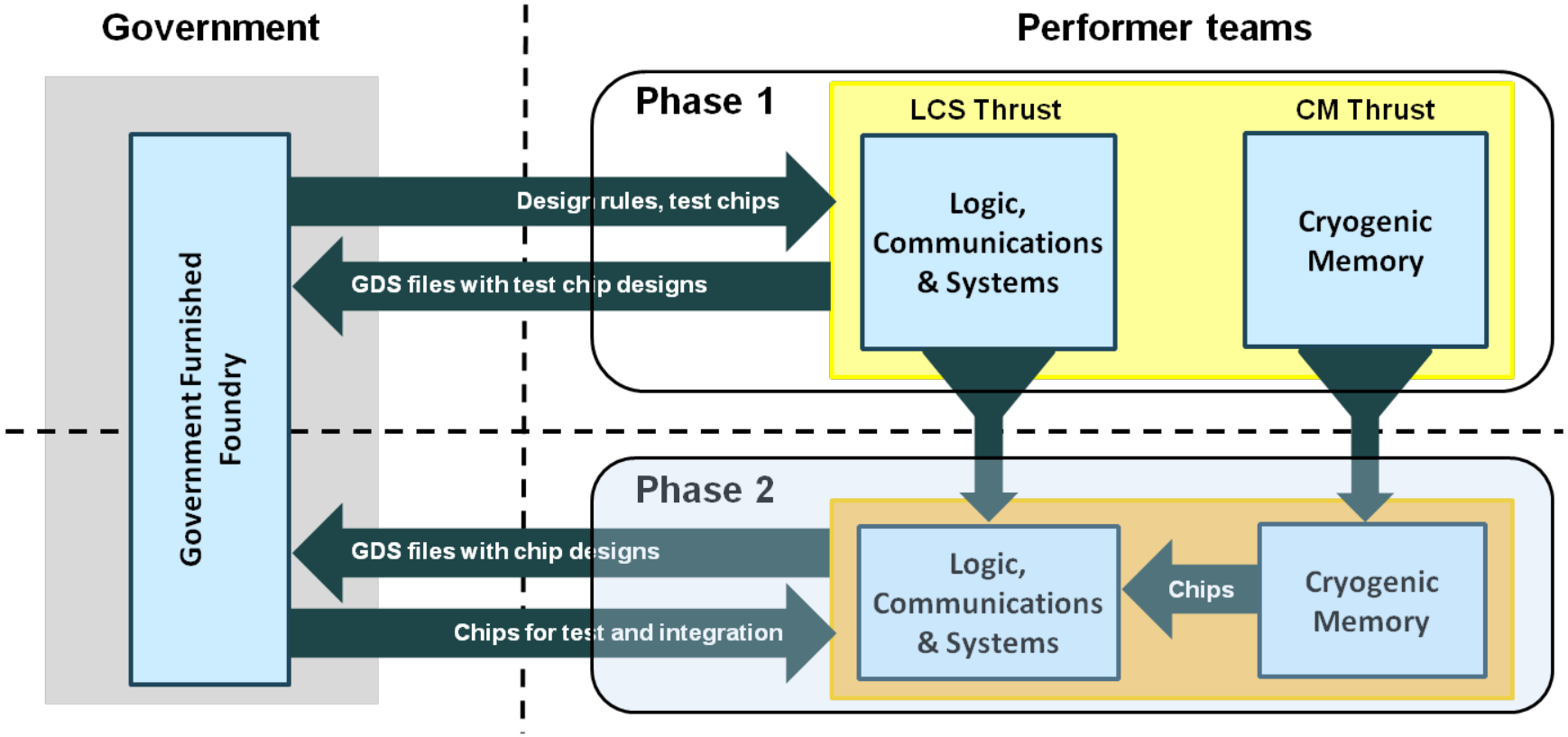
Metric	Goal
Clock rate for superconducting logic	10 GHz
Throughput (bit-op/s)	10^{13}
Efficiency @ 4 K (bit-op/J)	10^{15}
CPU count	1
Word size (bit)	64
Parallel Accelerator count	2
Main Memory (B)	2^{28}
Input/Output (bit/s)	10^{9}

Program Metrics and Goals

Metric	BP	OP1	OP2
Cryogenic Memory	Memory cell	Array	Chip
Functional capacity (bit)*	1	2^6 ; 2^6	2^{10} ; 2^{10}
Density (bit/cm^2)*	10^6 ; 10^5	$5x10^6$; $5x10^5$	10^7 ; 10^6
Data rate, burst mode (Gbit/s)*	1	5; 30	5; 30
Access time, ave. (ps)*	10,000; 1,000	5,000; 400	5,000; 400
Access energy, ave. (J/bit)*	5×10^{-16} ; 5×10^{-17}	5×10^{-16} ; 5×10^{-17}	10^{-16} ; 10^{-17}
Logic, Comm. & Systems	Subcircuits	Circuits	Processors
Benchmark circuits & applications	Circuits 1	Circuits 2	Circuits 3
Complexity (JJ)	10^4	5×10^4	10^5
Density (JJ/cm^2)	10^5	5×10^5	10^6
Throughput (bit-op/s)	10^9	5×10^{10}	10^{11}
Efficiency @ 4 K (bit-op/J)	10^{16}	5×10^{16}	10^{17}

* Memory metrics: The first number refers to Main Memory and the second to Cache Memory.

C3 Program Organization



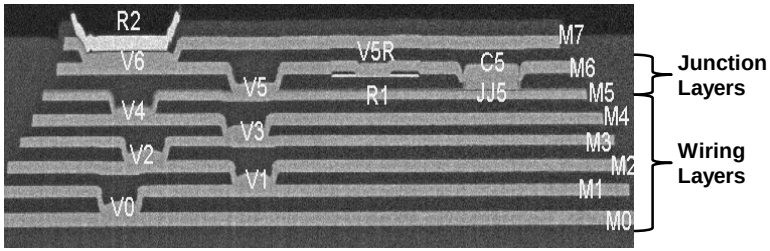
C3 Program Schedule

Period	Management Milestone	Month	Date
Phase 1 Base Period (BP)			
	Kickoff	0	07/29/2014
	Start Date	1	09/01/2014
	PI Meeting & Workshop	6	02/18/2015
	PI Meeting & Workshop	12	08/11/2015
	Program Review (decision on OP1)	14	11/05/2015
Phase 1 Option Period 1 (OP1)			
	PI Meeting & Workshop	18	03/10/2016
	PI Meeting & Workshop	24	08/10/2016
	Program Review (decision on OP2)	29	11/15/2016
Phase 1 Option Period 2 (OP2)			
	PI Meeting & Workshop	32	02/15/2017
	Decision on Phase 2 BAA release	34	04/15/2017
	PI Meeting & Workshop	38	08/15/2017
	Program Review (decision on Phase 2 follow-on)	41	11/15/2017

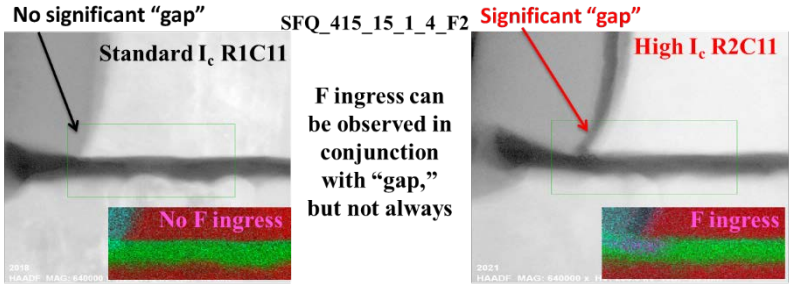
- Marc Manheimer, Program Manager
  - http://www.iarpa.gov/Programs/sso/C3/c3.html

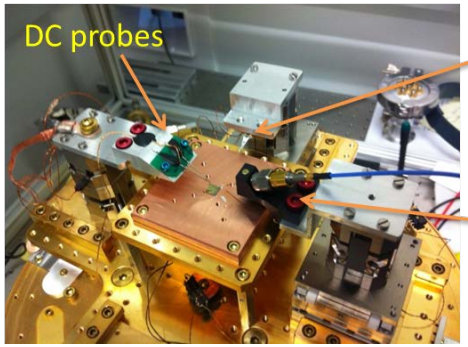
C3 Government Team

- MIT Lincoln Laboratory
  - Superconducting electronics foundry
  - Process development
- Sandia National Laboratories
  - Failure analysis
  - Superconductivity expertise
- NIST Boulder
  - Test & evaluation of performer circuits
  - Government program support
- NASA-JPL (contract pending)
  - Tunnel junction improvement



8 niobium layer cross-section





MIT-LL Superconducting Technology Roadmap

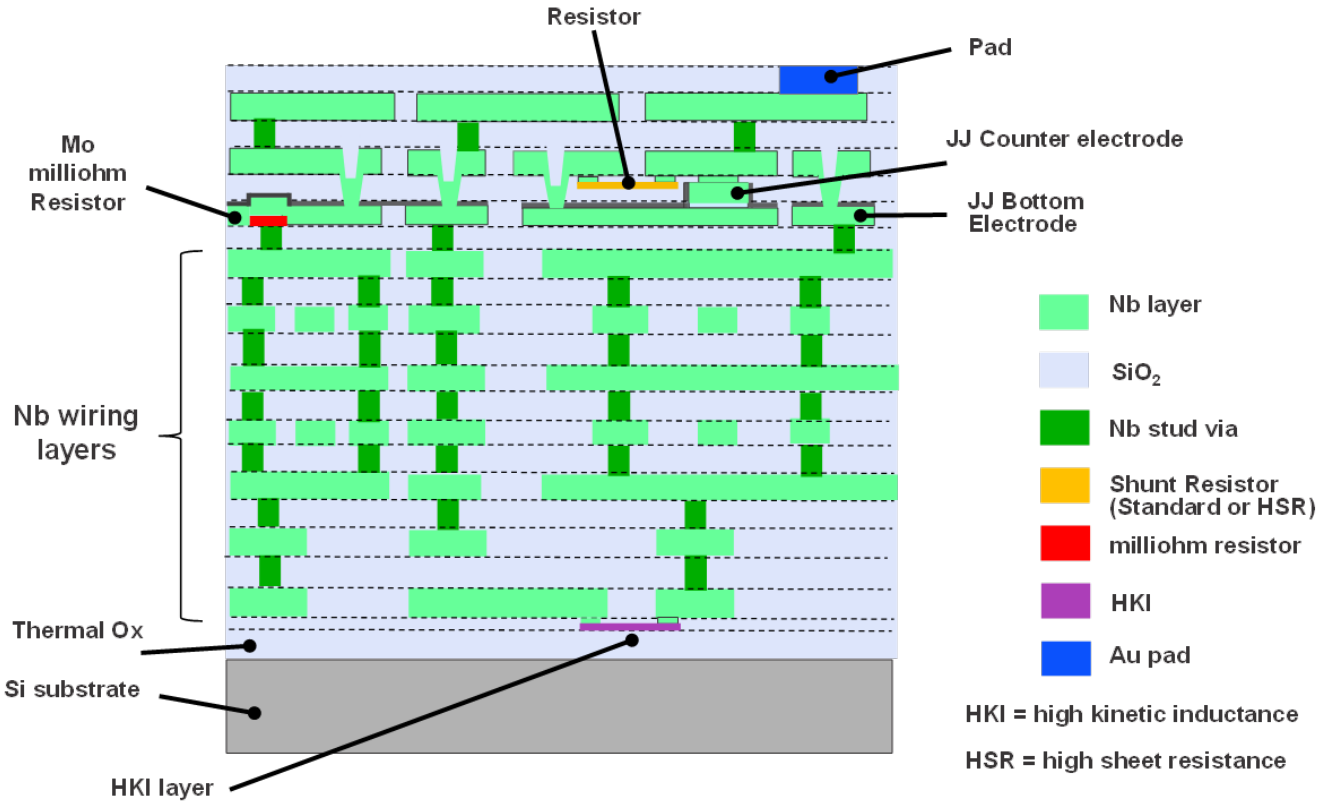
Fabrication Process Attribute		Units	Process Node					
			SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ7ee	SFQ8ee
Critical current density		MA/m^2	100	100	100	100	100	100
JJ diameter (surround)		nm	700 (500)	700 (500)	700 (300)	700 (300)	500 (200)	500 (200)
Nb metal layers		-	4	8	8	10	10	10
Line width (space)	Critical layers	nm	500 (1000)	500 (700)	350 (500)	350 (500)	250 (300)	180 (220)
	Other layers	nm			500 (700)	500 (700)	350 (500)	250 (300)
Metal thickness		nm	200	200	200	200	200	150
Dielectric thickness		nm	200	200	200	200	200	180
Resistor width (space)		nm	1000 (2000)	500 (700)	500 (700)	500 (700)	500 (500)	350 (350)
Shunt resistor value		Ω/sq	2	2	2 or 6	2 or 6	2 or 6	2 or 6
mΩ resistor		mΩ	-	-	3 - 10	3 - 10	3 - 10	3 - 10
High kinetic inductance layer		pH/sq	-	-	8	8	8	8
Via diameter (surround)		nm	700 (500)	700 (500)	500 (350)	500 (350)	350 (250)	350 (200)
Via type, stacking		-	Etched, Staggered	Etched, Stacked \2/	Etched, Stacked \2/	Etched, Stacked \2/	Stud, Stacked	Stud, Stacked
Early access availability		-		2014-09	2015-09	2016-03	2016-09	2017-09

Changes from the previous process

Microelectronics Lab,
MIT Lincoln Laboratory

- Nb/Al-AlOx/Nb JJ technology
- 200 mm Si wafers, full planarization

SFQ7ee process node (2016)

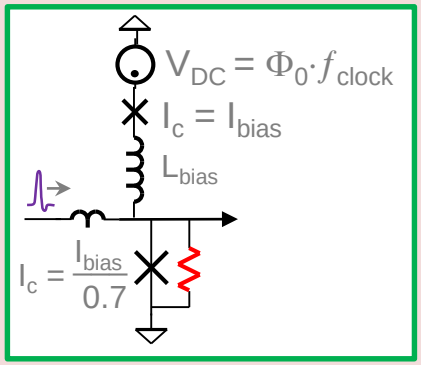


- 10 Nb layers, 250 nm minimum wire width, 300 nm spacing
- 500 nm minimum junction dia., J_C target: 100 $\mu A/\mu m^2$

Logic Communications & Systems: 2 Projects

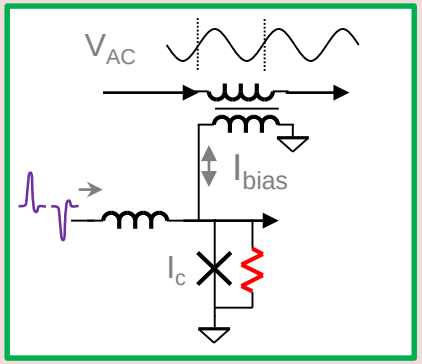
- **IBM** team (Gerald Gibson)
  - Architecture: many lightweight processors
  - ERSFQ/eSFQ circuit families (Hypres)
    - DC power, zero static power dissipation
    - "1": single SFQ pulse; "0": no pulse

ERSFQ (power: – dc)



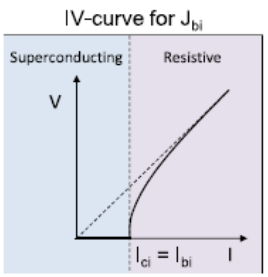
- **Northrop Grumman** team (Quentin Herr)
  - Architecture: RISC processor
  - Reciprocal quantum logic (RQL) circuit family
    - RF clock and power (~ 10 GHz)
    - "1": pair of reciprocal SFQ pulses; "0": no pulses

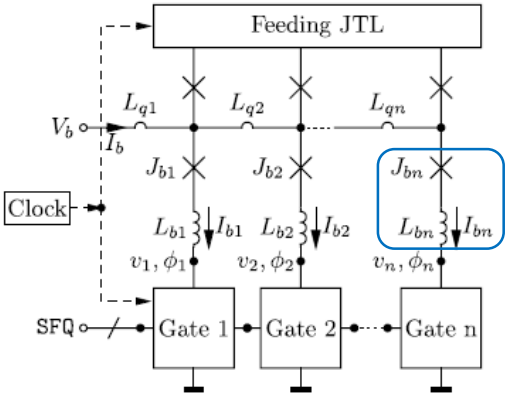
RQL (power: ~ ac, 10 GHz)

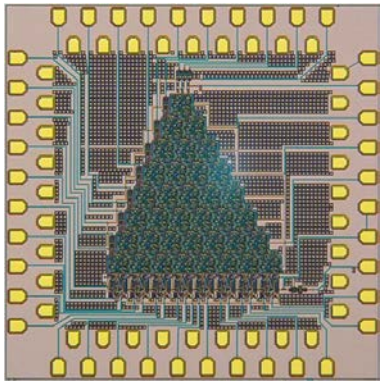


Energy-Efficient SFQ (eSFQ, ERSFQ)

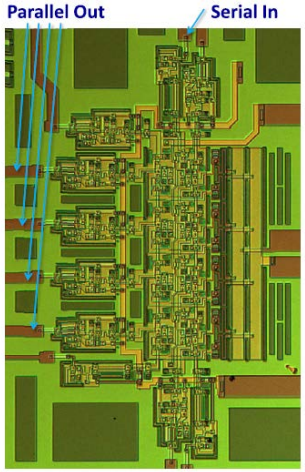
- SFQ logic families developed at Hypres
  - DC supply current, zero static power dissipation using a JJ and large inductor in series
  - Clocked by SFQ pulses distributed separately
  - ERSFQ and eSFQ can be combined in a single circuit
- Demonstration circuits:
  - ERSFQ 8-bit adder (2011)
    Kirichenko et al. IEEE Trans. Appl. Supercond. (2011)
  - 0.8 aJ/bit eSFQ circuit
    Volkmann et al. Supercond. Sci. Tech. (2013)







ERSFQ 8-bit adder



eSFQ shift register and deserializer test circuits

Mukhanov, IEEE Trans. Appl. Supercond. (2011)

Record 415 GHz Toggle Flip-Flop

IBM

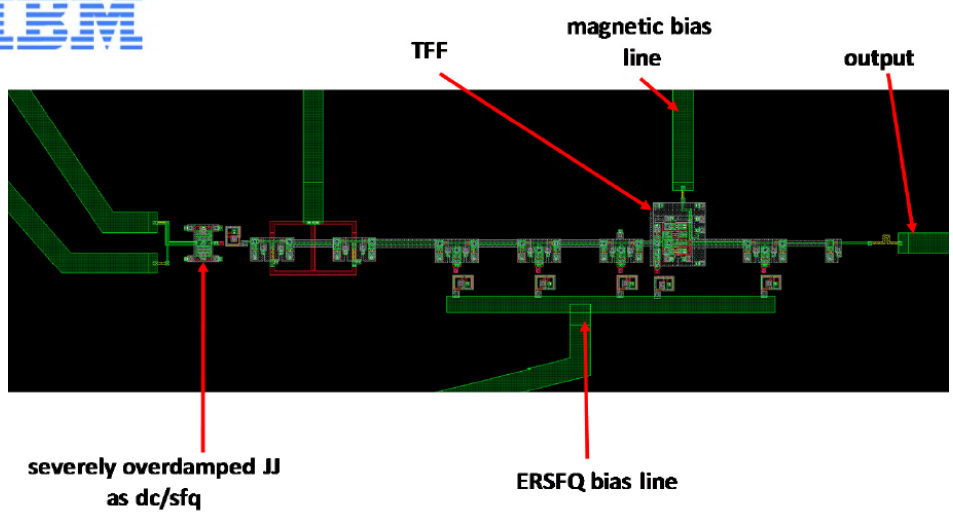
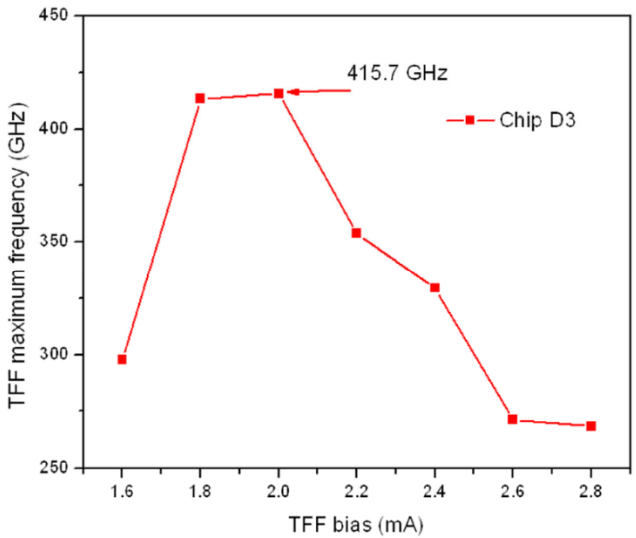


Figure 7: TFF-based Static Frequency Divider Circuit



2015-01-IBM Technical MSR

- 415 GHz maximum operating frequency of a toggle flip-flop (TFF) circuit was demonstrated, a **record** for Josephson junctions with critical current density J_c = 135 MA/m^2.
- ERSFQ is an energy-efficient superconducting digital circuit family, proving that both high speed and high efficiency are possible in the same circuit.

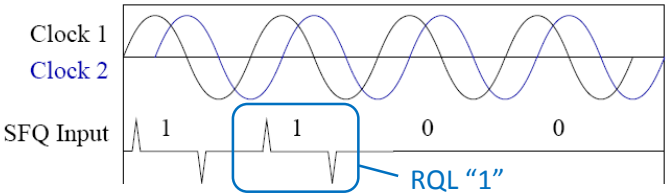
NORTHROP GRUMMAN

RQL 8-bit Kogge-Stone Adder

- Carry look ahead adder (CLA) core
  - Excluding: input shift registers, output amps
  - Fabricated in Hypres 45 MA/m^2 process

JJs	815
Ave I_C	162 μA
Clock	6.2 GHz
Power	560 nW @ 6.2 GHz with 1.2 mW clock
Energy	~5x10^{-5} pJ
Latency	150 ps @ 10 GHz
Area	~ 4 mm^2

- Projected 64-bit adder in advanced process: 100 ps latency at 20 GHz with 1.2 mW clock



Q. Herr et al., J. Appl. Phys. (2011)

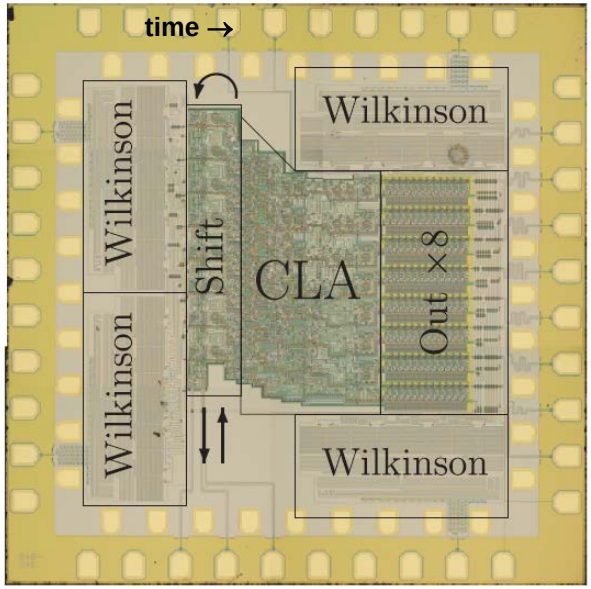


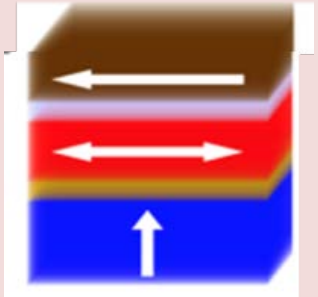
FIG. 3. Picture of the fabricated 8-bit CLA on a 5 mm die, using a 2 μm superconducting Nb process.

A. Herr et al., J. Appl. Phys. (2013)

Cryogenic Memory: 2 Projects

- **Raytheon BBN** team (Tom Ohki)
  - Orthogonal STT memory (Andrew Kent, NYU)
  - Spin Hall effect memory (Robert Buhrman, Cornell U)
  - nTron drivers or memory elements (Karl Berggren, MIT)
  - eSFQ/ERSFQ logic circuits (Hypres)

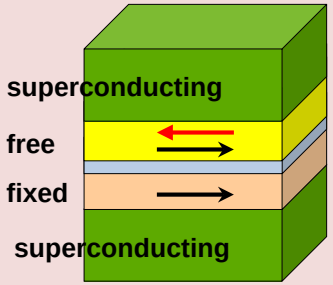
COST-MRAM



Power:
DC —

- **Northrop Grumman** team (Anna Herr)
  - Spin valve devices (Nathan Newman, ASU)
  - Spin valve materials (Norman Birge, MSU)
  - Fabrication process development (Jiwei Lu, UVA)
  - RQL logic circuits (NGC)

JMRAM

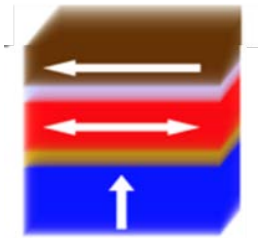


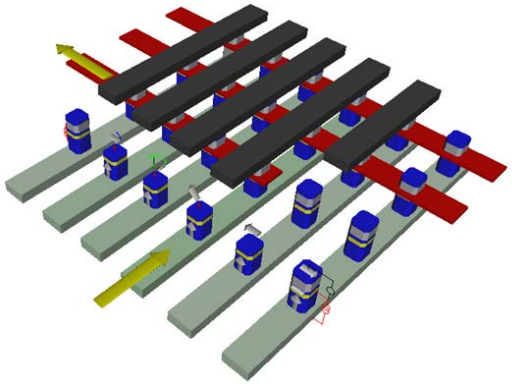
Power:
AC ~
10 GHZ

COSTRAM: Cryogenic Orthogonal Spin Transfer RAM

Raytheon
BBN Technologies

- Raytheon BBN, NYU (Andy Kent), Hypres
- Memory element
  - Write current through element, not field lines
  - 3 to 4% MR
  - No thermal fluctuations required
  - <100 ps switching times
- Logic
  - ERSFQ or eSFQ (Hypres)

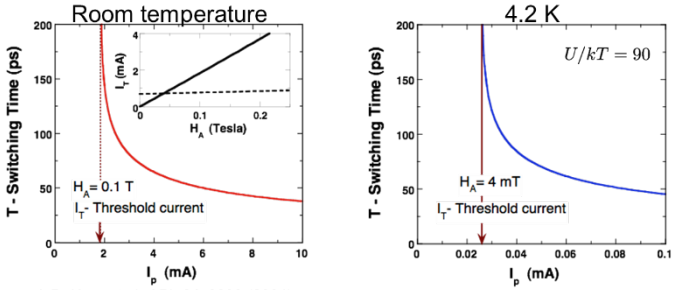




Optimization for Low Temperature

- OST-MRAM operates at low temperature: thermal fluctuations are **not needed** to initiate switching events
- Current required to write bit cell at low temperature is greatly reduced

$I_T \propto U$ for long-term stability: $U/kT > 60$



A.D. Kent *et al.*, APL **84**, 3899 (2004)

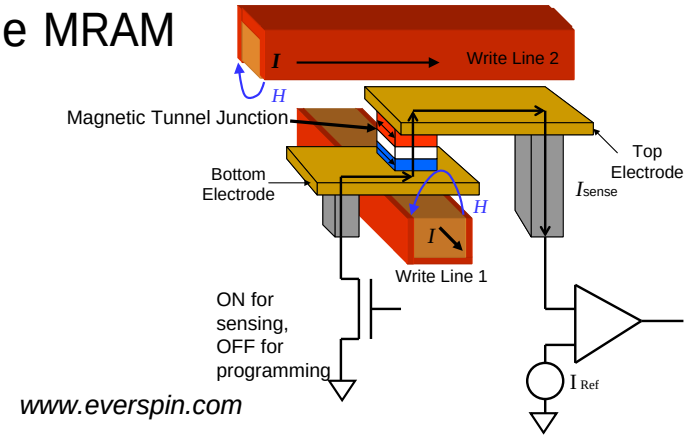
- Write energy estimate: $E = I^2 R\tau \simeq 10^{-19}$ J
- Read energy estimate: $E = 10^{-20}$ J

L. Ye et al., "Spin-transfer switching of orthogonal spin-valve devices at cryogenic temperatures," JAP (2014)

NORTHROP GRUMMAN

JMRAM: Josephson MRAM

Toggle MRAM



www.everspin.com

- Memory cell: Josephson junctions with magnetic tunnel barriers
  - Physics demonstrated in SFS JJs
  - Memory state: high or low I_c
  - Write: magnetic field switching of the “soft” magnetic layer
  - Read: Josephson effect
- No static power dissipation
- Read energy dissipated only for logical “1”

Superconducting Computing and the IARPA C3 Program

- Problems in large scale computing
- Feasibility study
- Cryogenic Computing Complexity (C3) program (IARPA)
- Challenges
- Related work
- Conclusions

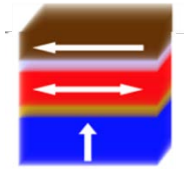
Challenges

- Fabrication } Subject of next talk
- Memory
  - Magnetic memory device physics and fabrication
  - Cell size
- Superconducting circuit physics
  - Coupled current and inductance
  - Low gain from JJs
- Electronic design automation (EDA) tools
- Input/Output
  - Optical needed
  - High-speed, low heat leak
- Circuit complexity, density
- Cryogenic and (non-) magnetic environment
  - Materials and packaging
  - Refrigeration

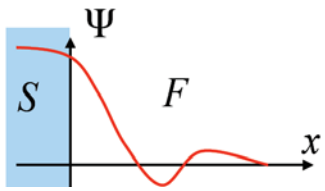
} Future

Challenges: Memory

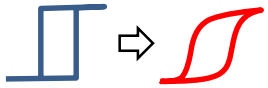
#1



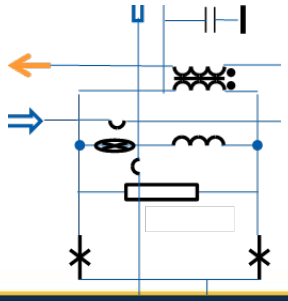
- Variety of device types with no clear winner
  - Magnetic spin valve (SV), spin Hall effect (SHE), spin-transfer torque (STT), …
  - New materials: NiFeMo, NiFeCu, NiFeNb, Co/Ru/Co, $[Co/Ni]_n$, …
  - New physics combining spintronics and superconductivity

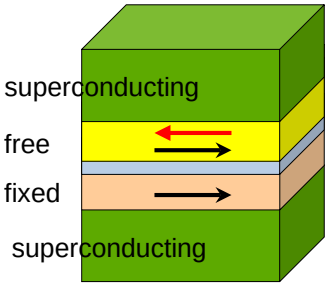


- Process control
  - Low energy operation and superconductivity demand thin layers
  - Thickness (~ 1 nm) exponentially affects device parameters
  - Interfacial roughness degrades properties and increases spreads
  - Properties change from room temperature to 4 K



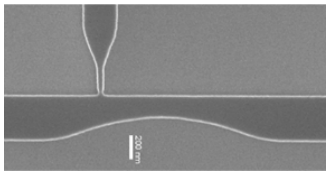
- Memory cell size
  - Multiple devices per cell
  - No equivalent to DRAM yet



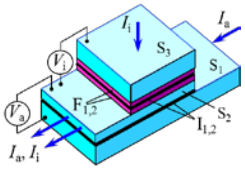


Challenges: Superconducting Circuits

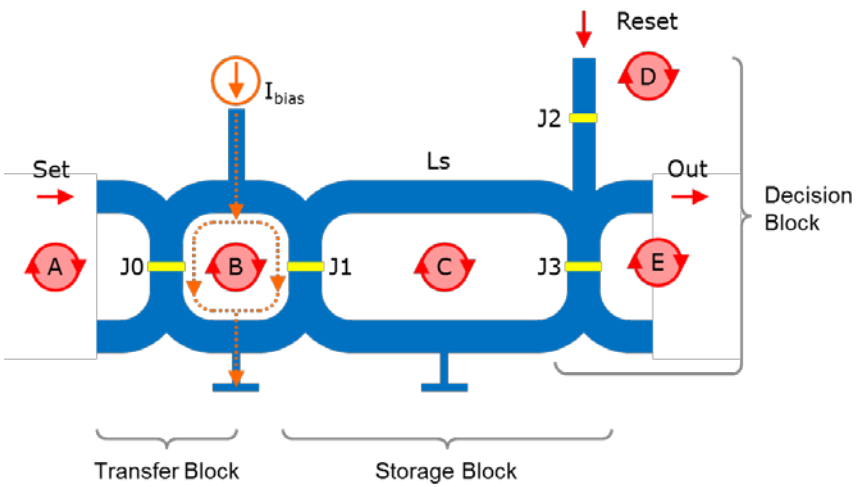
- Inductance (***L***) and critical current (***I***$_c$) are linked for SFQ circuits
  - SFQ: Single Flux Quantum, Φ_0 = 2.07 fWb (mV·ps or mA·pH)
  - Flux: $I \cdot L = \Phi = \alpha\Phi_0 \approx \Phi_0$ **required for circuit operation**!
  - Switching energy: $E_{sw} = I_c \cdot \Phi_0$
  - Decreasing I_c (more energy efficient!) requires increasing ***L***
- Low gain
  - Fan-out > 1 requires splitters
  - Low gain from Josephson junctions (3 JJs to make a 2:1 splitter)
  - Low isolation across JJs
  - Alternatives are being explored



3-terminal nanowire switch



S-F transistor

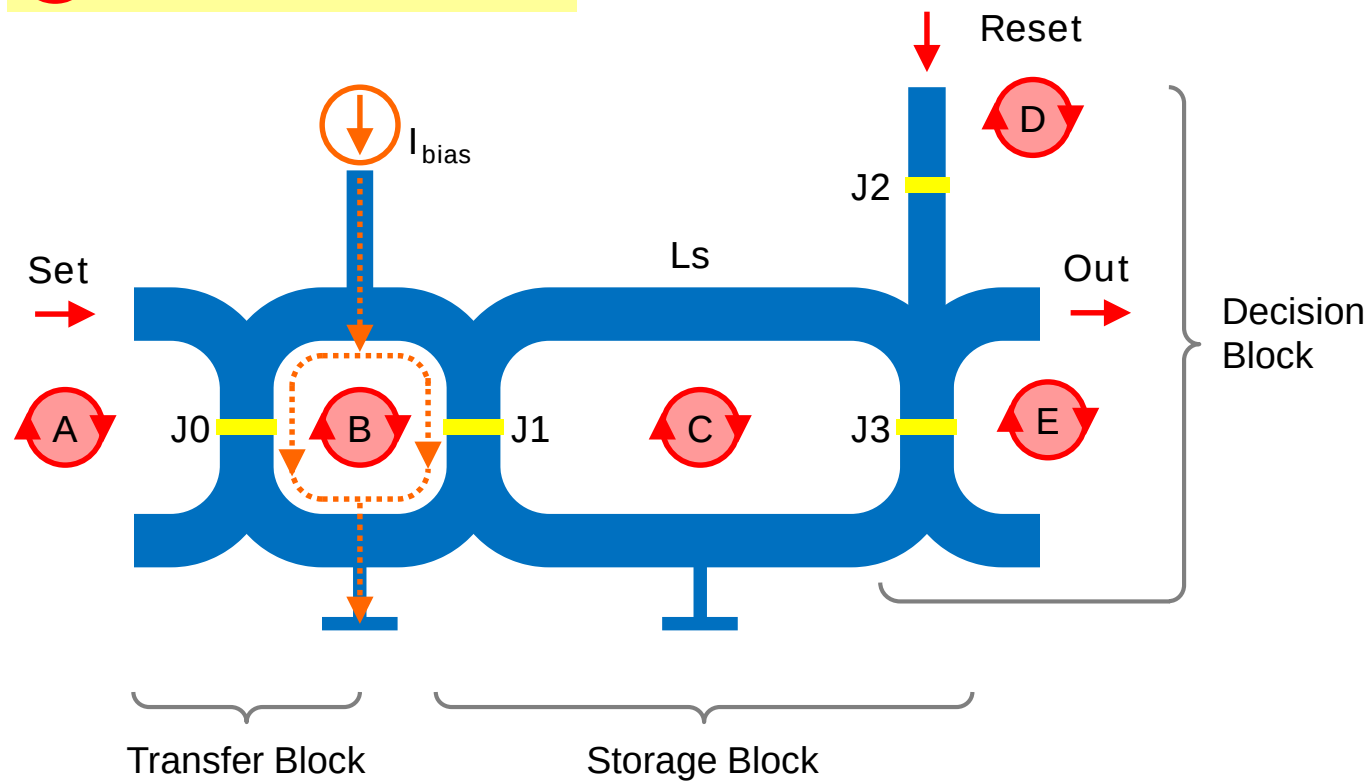


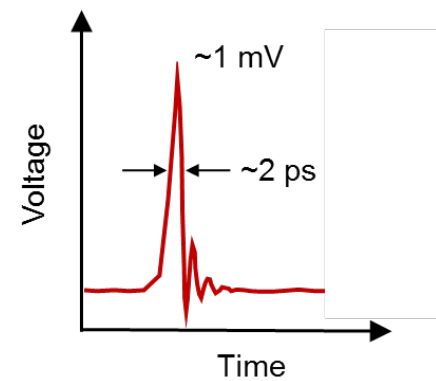
Holmes, Kadin, Johnson, *Computer*, Dec. 2015

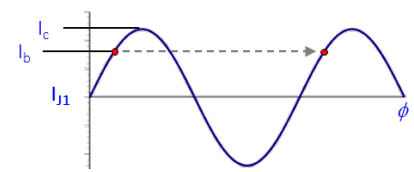
SFQ gate: set-reset (SR) flip-flop

Single Flux Quantum (SFQ)

$I \cdot L = \Phi_0 = 2.07$ mA·pH

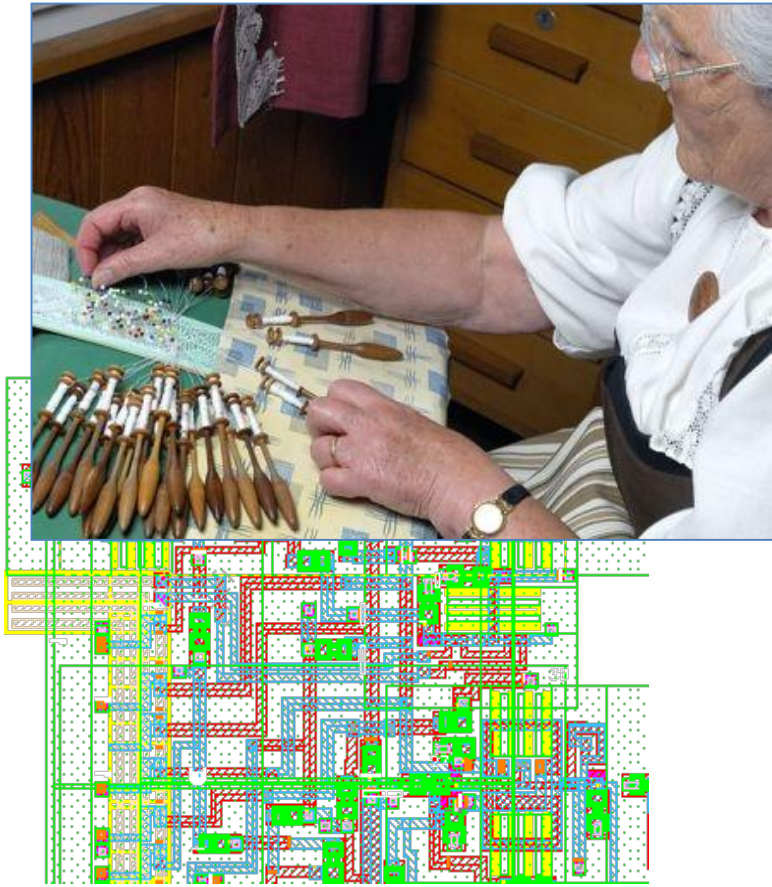






Challenges: EDA and Designers

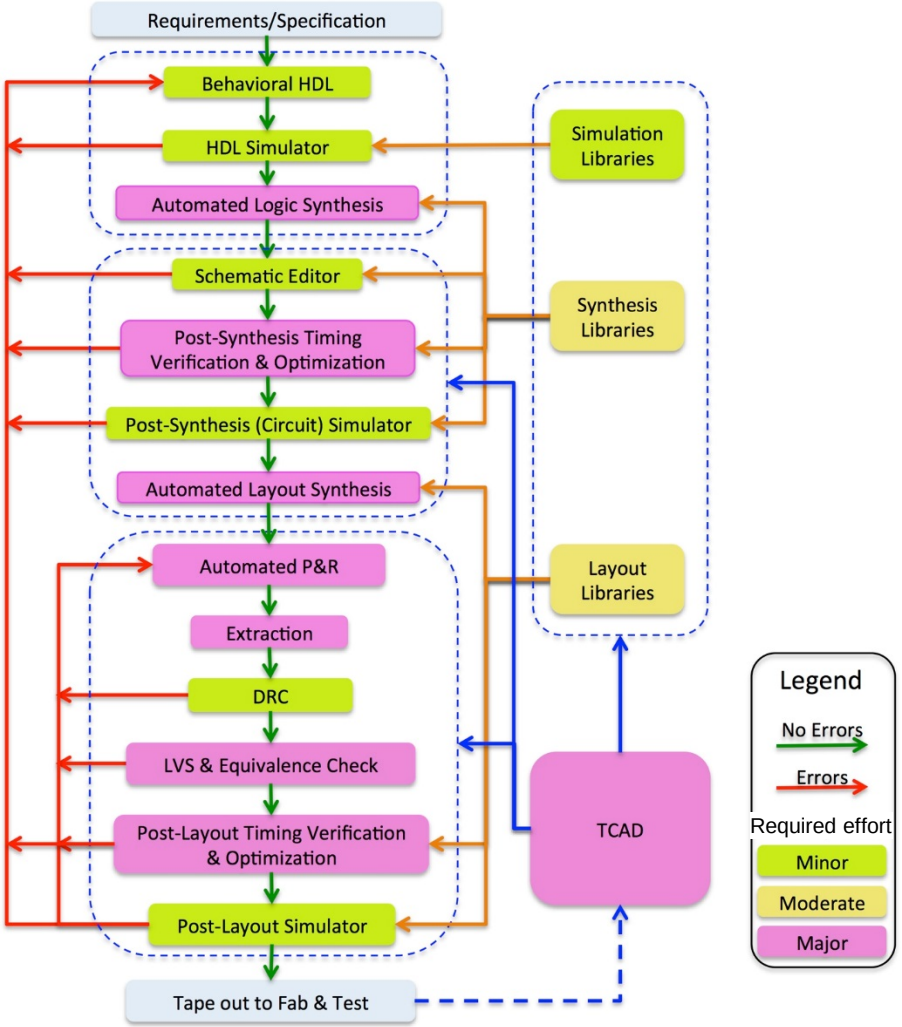
- Electronic design automation (EDA) tools missing or needing improvement:
  - Inductance extraction
  - Placement and routing (inductance range)
  - Synthesis
  - Timing analysis
  - Simulation
  - PDKs (not provided by foundry!)
- SFQ designers
  - No classes in the USA
  - Few designers



"Manual design is like making lace." (SFQ designer)

SCE EDA Tool Status

- Design, analysis, and verification tools need to be developed into a comprehensive EDA tool set specific to very large scale superconducting integrated circuits.



SCE = Superconducting Electronics
EDA = Electronic Design Automation
HDL = Hardware Description Language
P&R = Place-and-Route
DRC = Design Rule Check
LVS = Layout versus Schematic
TCAD = Technology CAD

SuperTools Program (IARPA)

- **Request for Information** (Posted 2015-01-12)
  Electronic Design Automation tools for Superconducting Electronics (EDA for SCE)
  http://www.iarpa.gov/index.php/working-with-iarpa/requests-for-information/electronic-design-automation-tools-for-superconducting-electronics

- **Proposers' Day** (2016-02-10)

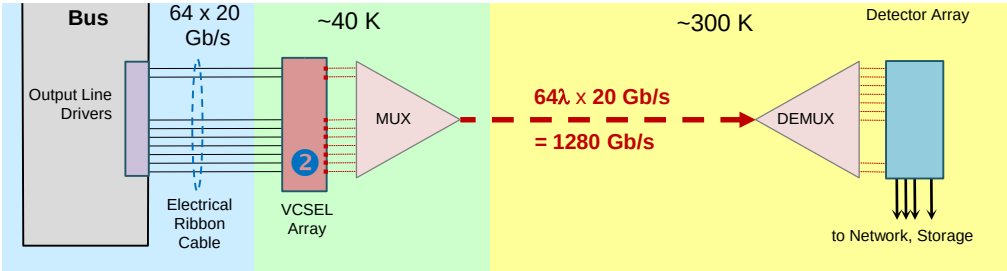
- Broad Agency Announcement (BAA) in process

- Mark Heiligman, Program Manager

Cryo-to-Room Temperature Interconnects

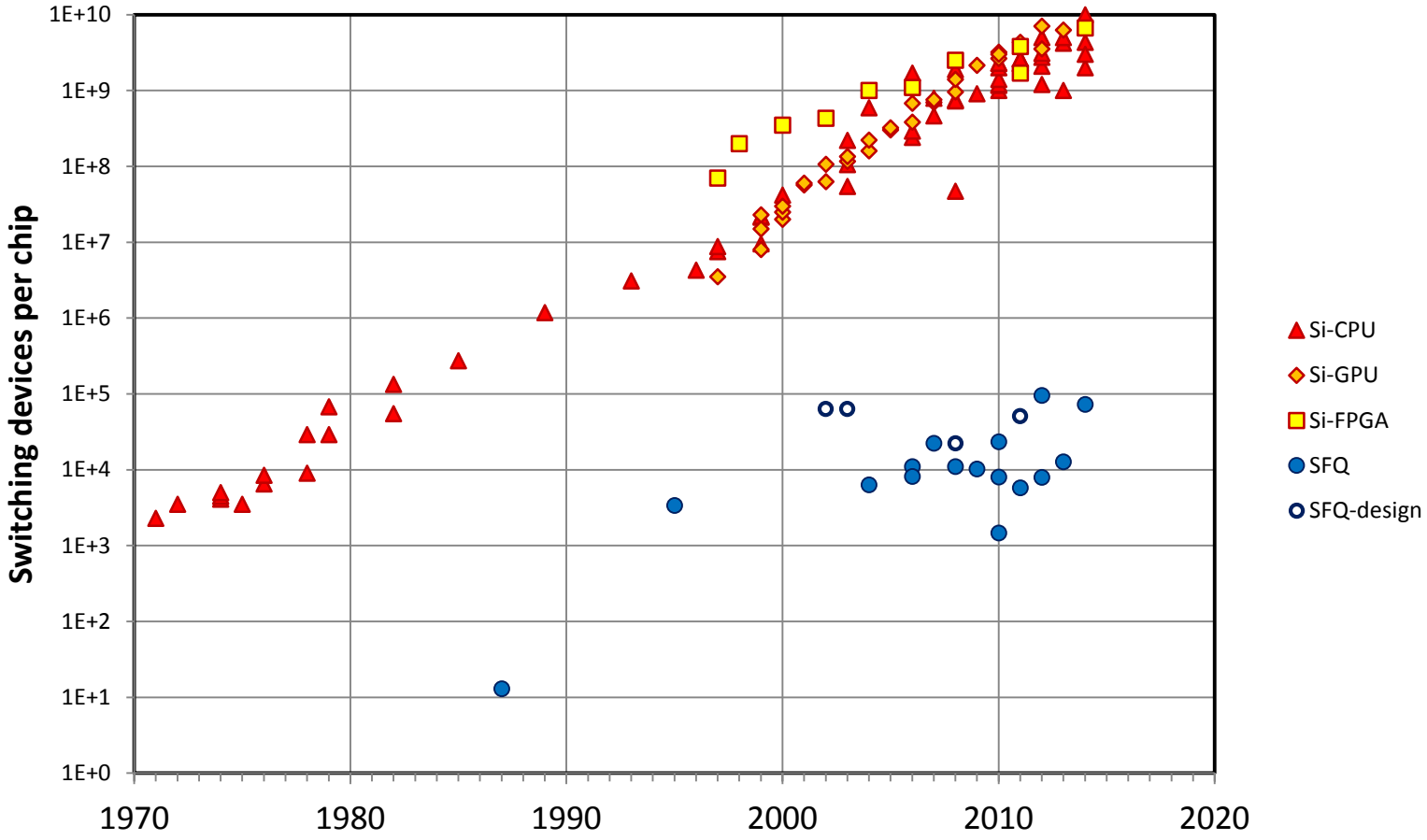
- Electrical interconnects allow heat into the cryogenic environment

- Optical interconnects are preferred
  - SFQ energy: $E_{SFQ} = I_c \cdot \Phi_0$ = (0.1 mA)(2.07 mV·ps) = 2.1×10^{-19} J = 0.21 aJ
  - Photon energy: $E_{ph} = hc/\lambda$ = (6.6e–34 Js)(3e+8 m/s)/(1550 nm) = 0.13 aJ
  - In is easier, as there are typically many photons per bit
  - Out is 'IARPA hard'

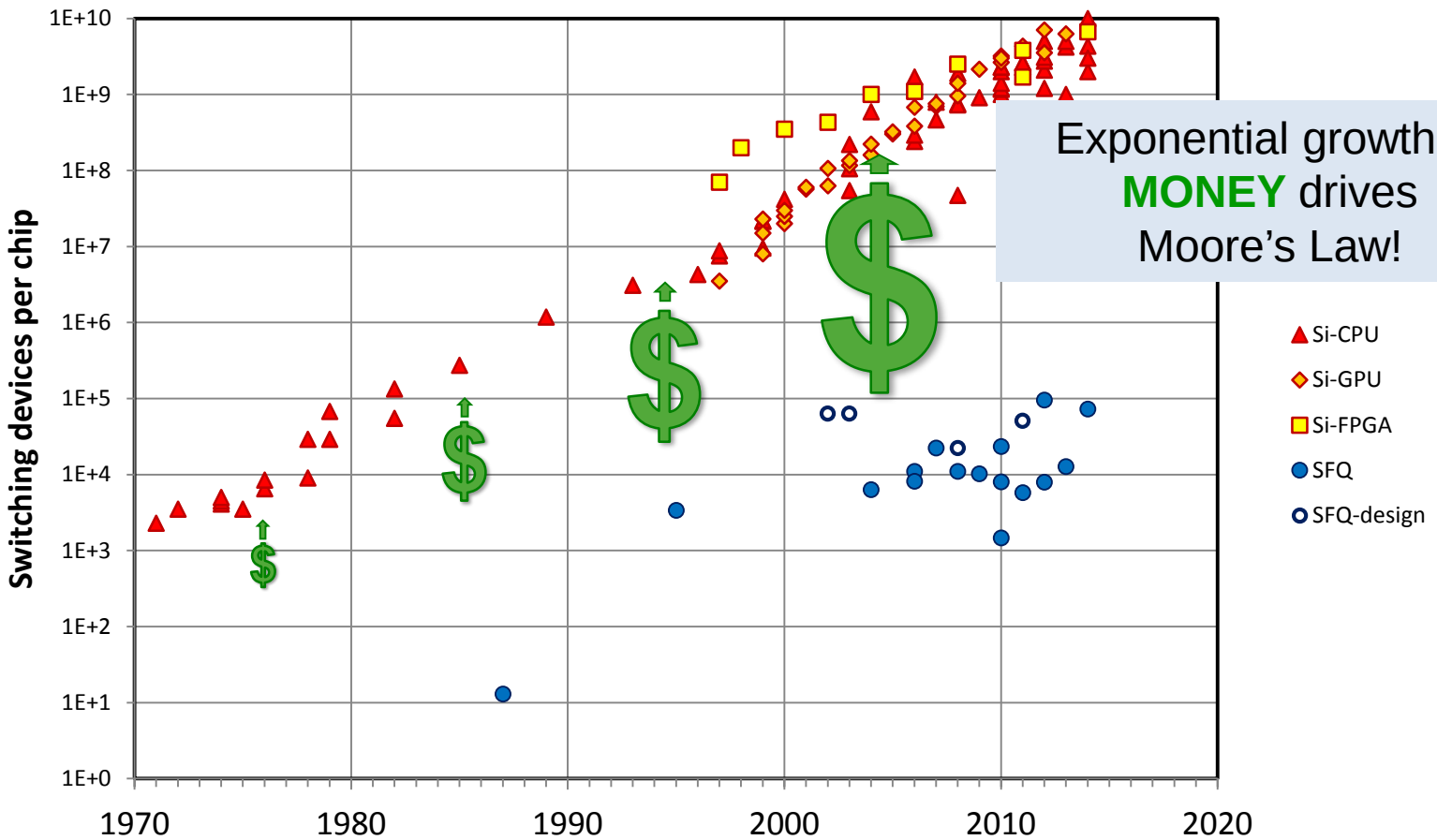


- **Request for Information** IARPA-RFI-16-04 (posted 2016-01-28)
  Data Ingress and Egress for Cryogenic Systems
  http://www.iarpa.gov/index.php/working-with-iarpa/requests-for-information/data-ingress-and-egress-for-cryogenic-systems

Complexity: SFQ lags semiconductors by ~ 10^5



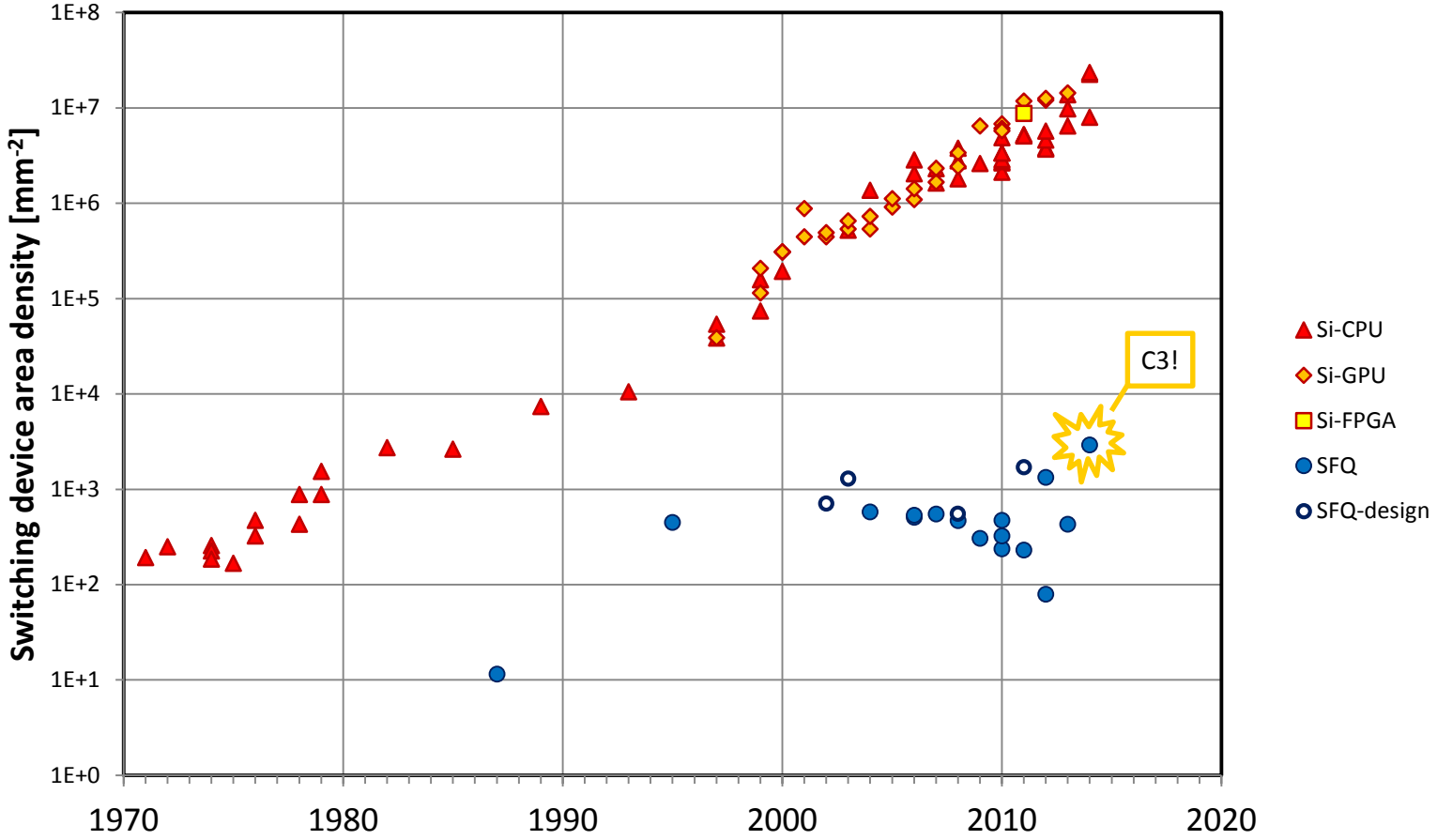
Complexity: SFQ lags semiconductors by ~ 10^5



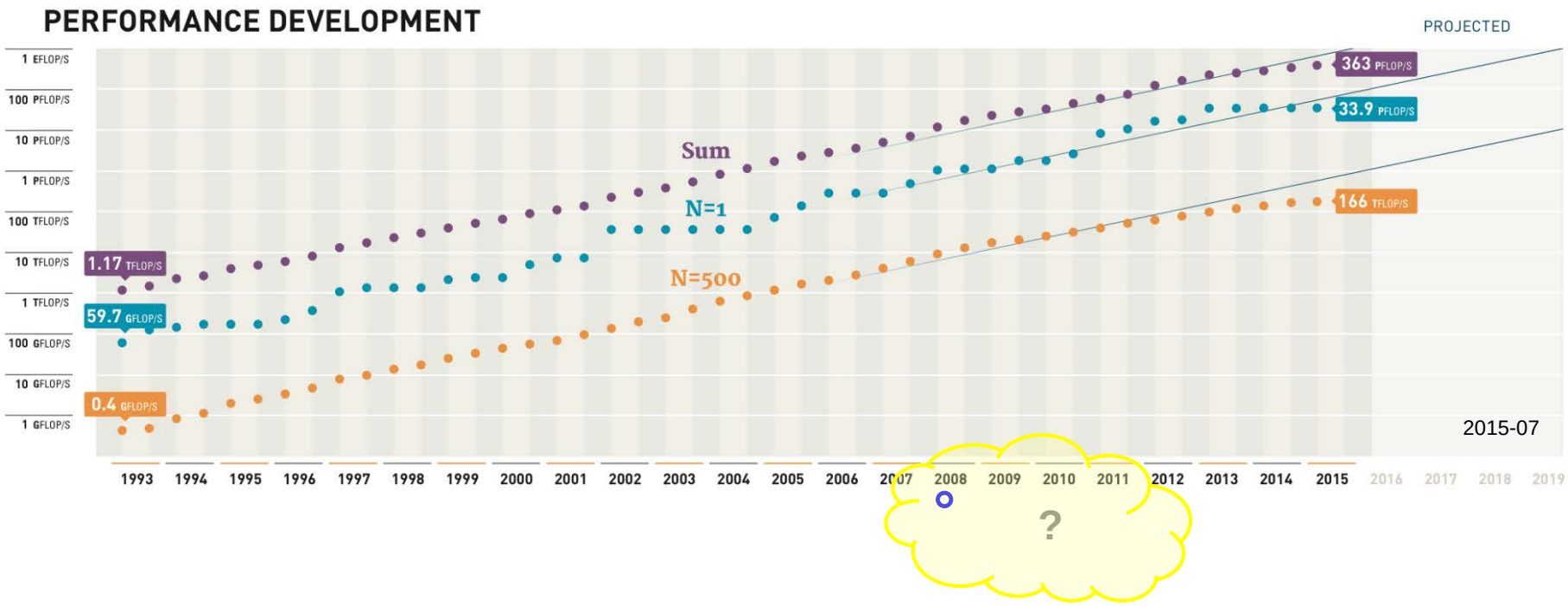
Exponential growth in **MONEY** drives Moore's Law!

Nagy et al. (2013) **Statistical Basis for Predicting Technological Progress**. PLoS ONE 8(2): e52669

Density: SFQ lags semiconductors by ~ 10^4



System performance lags by ≈ 10^{10}



- But comparison is difficult – no superconducting computer has run a LINPACK benchmark to measure performance in FLOP/s

Can superconducting computing compete?

Shadow of the Colossus/
Wander to Kyozō
SCEI

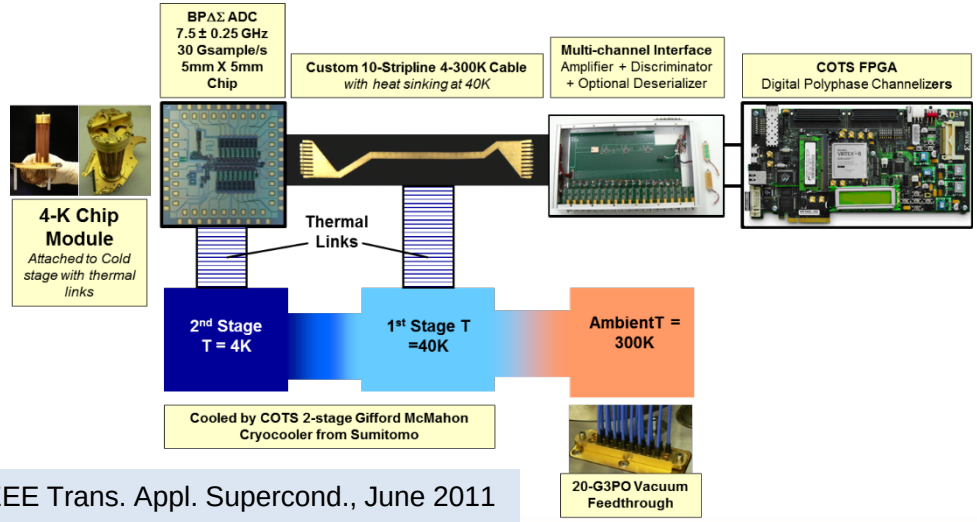
A better way to view the relationship

Superconducting Computing and the IARPA C3 Program

- Problems in large scale computing
- Feasibility study
- Cryogenic Computing Complexity (C3) program (IARPA)
- Challenges
- Related work
  - Digital-RF Receiver (Hypres)
  - Quantum Annealing (D-Wave Systems)
  - Japanese Superconducting Computing Program
  - National Strategic Computing Initiative (NSCI)
  - SuperTools, Cryo-to-RT Interconnect Programs (IARPA)
- Conclusions

Digital-RF Receiver (Hypres)

- Commercial product with applications in:
  - Software-defined radio, satellite communications
- Directly digitizes RF (no analog down-conversion)
  - Ultra-wide bandwidth, multi-band, multi-carrier
- Hybrid temperature heterogeneous technology
  - Different technologies between ambient and 4 K
  - Closed-cycle cryogenic refrigerator

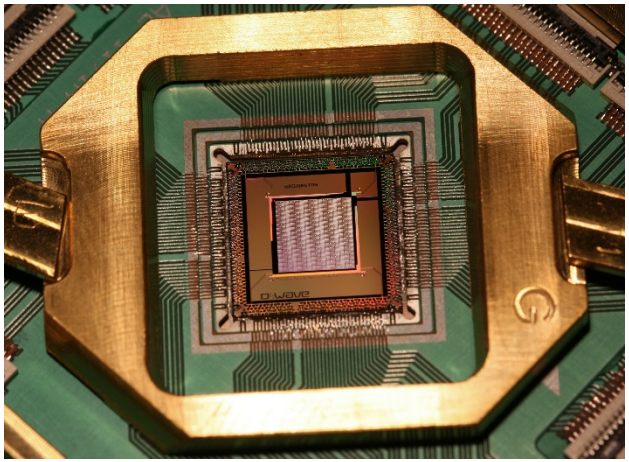


Gupta, et al., IEEE Trans. Appl. Supercond., June 2011

48 in.
rack

Quantum Annealing (D-Wave Systems)

- D-Wave® TwoX™ (2015 August 20), a commercial superconducting quantum annealing processor
- 128,000 Josephson junctions
- 1000 qubit array
- 15-20 mK operating temperature

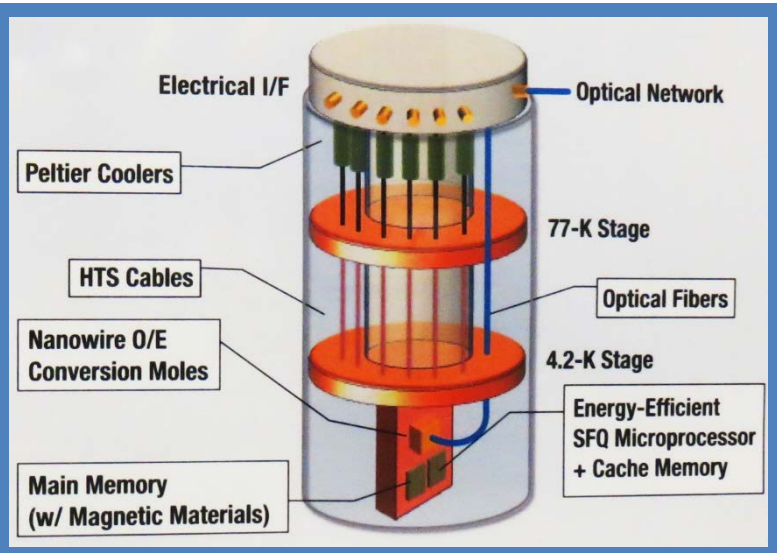


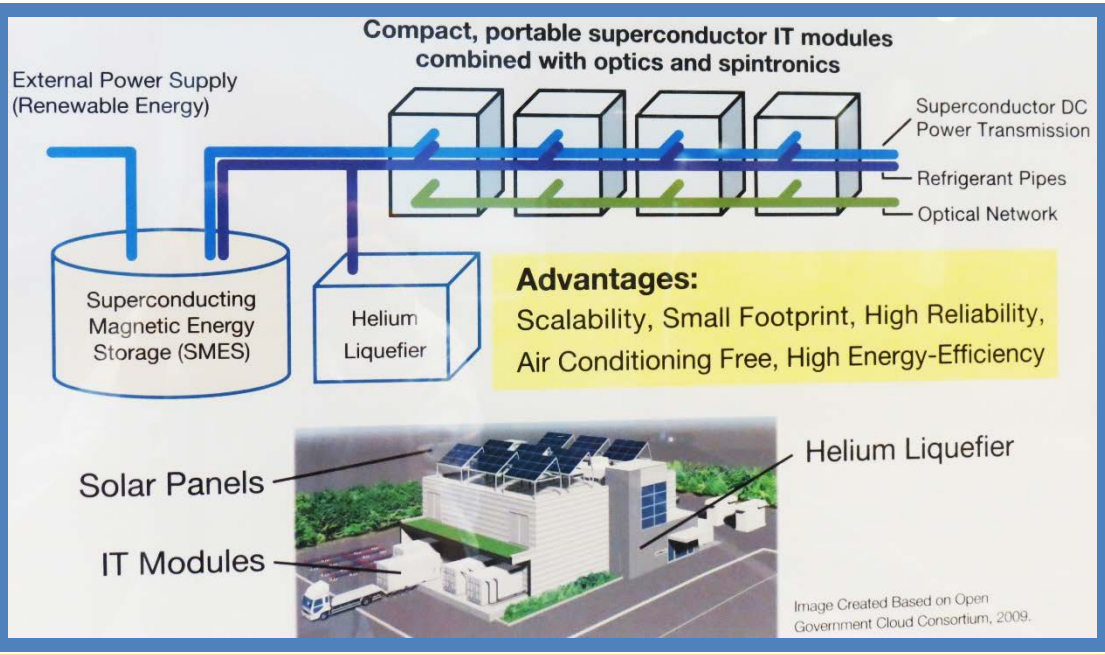
"Washington" chip

D-Wave® TwoX™ quantum annealing processor

Japanese 3-year program started

- "Superconductor Electronics System Combined with Optics and Spintronics" JST-ALCA Project: http://www.super.nuqe.nagoya-u.ac.jp/alca/ (Japanese)
- Processor goals: AQFP majority logic, 8-bit simplified RISC architecture, ~25,000 JJs, ~10 instructions





National Strategic Computing Initiative (NSCI)

Executive Order July 29, 2015

By the authority vested in me as President by the Constitution and the laws of the United States of America, and to maximize benefits of high-performance computing research, development, and deployment, it is hereby ordered as follows:

- (b) Foundational Research and Development Agencies. **There are two foundational research and development agencies for the NSCI**: the Intelligence Advanced Research Projects Activity (**IARPA**) and the National Institute of Standards and Technology (**NIST**).

IARPA will focus on future computing paradigms offering an alternative to standard semiconductor computing technologies. NIST will focus on measurement science to support future computing technologies. The foundational research and development agencies will coordinate with deployment agencies to enable effective transition of research and development efforts that support the wide variety of requirements across the Federal Government.

Superconducting Computing and the IARPA C3 Program

- Problems in large scale computing
- Feasibility study
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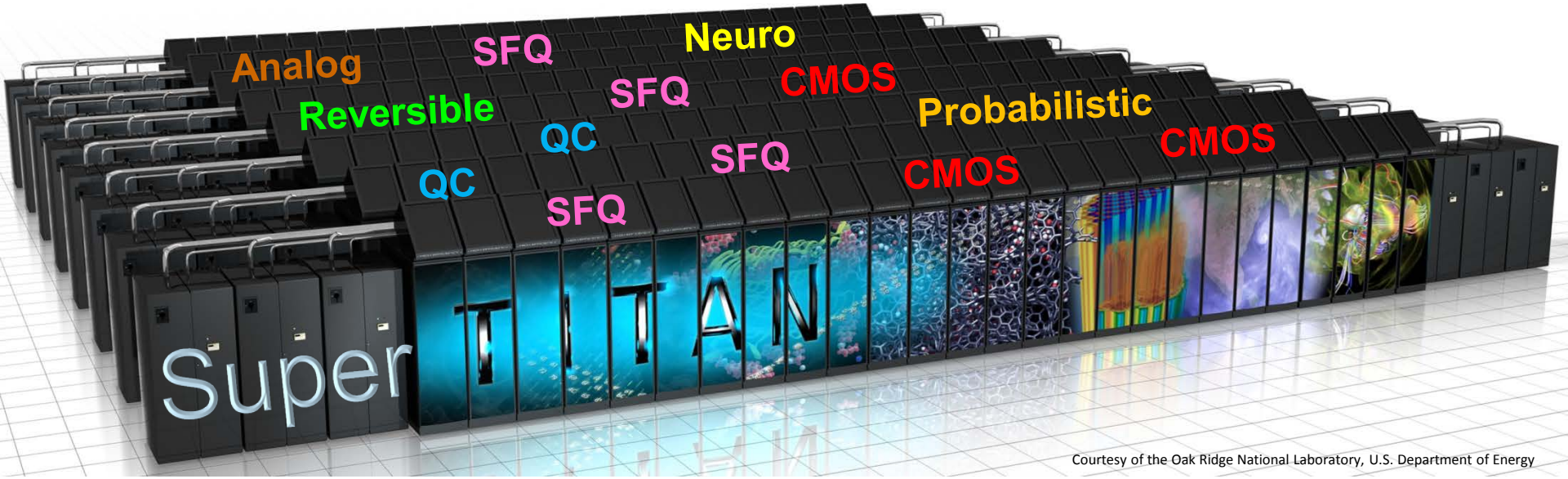
- Related work
- Conclusions

Future Supercomputing Vision



Courtesy of the Oak Ridge National Laboratory, U.S. Department of Energy

- Hybrid technologies: digital (CMOS, SFQ), probabilistic, analog, neuromorphic, reversible, and quantum computing (QC)
  — whatever works best!
- SFQ digital platform supports multiple cryogenic technologies
- Requires optical interconnects between room temperature and cryogenic nodes

Lessons from an Emerging Technology

- Fair **metrics** are needed to evaluate alternative computing technologies
  - level the playing field to allow different technologies to compete
  - relevant lessons from hiring for diversity?

- Ramping up requires time **and resources**
  - the real Moore's Law

- Government funding alone is not sufficient
  - cost to develop energy-efficient, large-scale computers is large
  - ramp up using smaller products and markets
- Don't go it alone
  - use your mother elephant

- Go big or go home!
  - small improvements are not worth the effort
  - large disruptions require even larger advantages

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Superconducting Computing in Large-Scale Hybrid Systems

D. Scott Holmes, Booz Allen Hamilton
Alan M. Kadin, Senior Member of IEEE
Mark W. Johnson, D-Wave Systems

Once focused solely on computation speed, superconducting computing is now proving useful in hybrid systems where its unique capabilities complement conventional computing technologies. Energy efficiency has become a strong motivation for developing large-scale superconducting systems.

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