Single Flux Quantum (SFQ) Circuit Fabrication and Design: Status and Outlook

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ORNL Beyond CMOS Workshop

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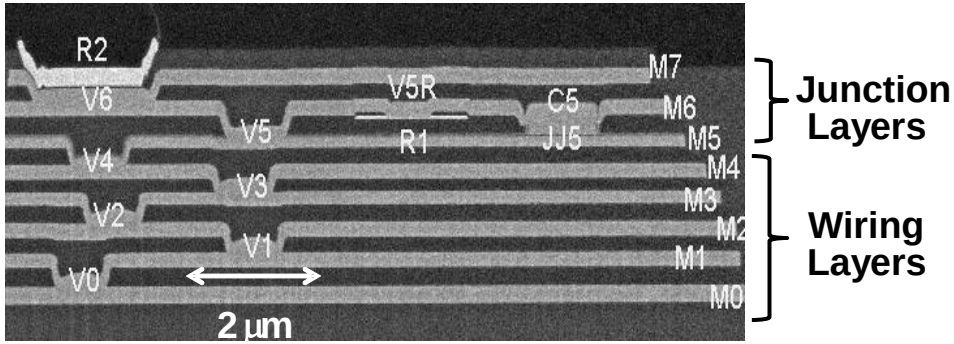
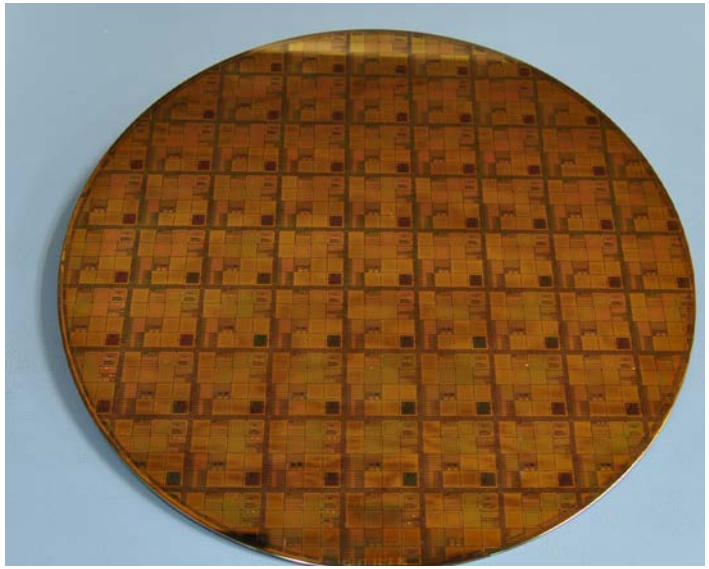
SFQ Fab is Not Dumbed-Down CMOS Fab

- **Looks easy! 1990's CMOS backend**
  - Feature sizes > 0.25 μm
  - 8 metal layers
  - Etched vias
  - No CMOS front end
- **Only needs 1990's tool set**
  - Sputtering tool
  - Dielectric deposition
  - CMP
  - Plasma etch tool
  - 248-nm lithography tool
- **But it is not**
  - Circuit performance critically dependent on component values
  - Metal & dielectric thickness to < 10%
  - Junction uniformity < 1% (1σ)
  - Process temperatures < 150 °C
  - Hydrogen incorporation is pernicious

Cross Section of MIT-LL SFQ4ee Process



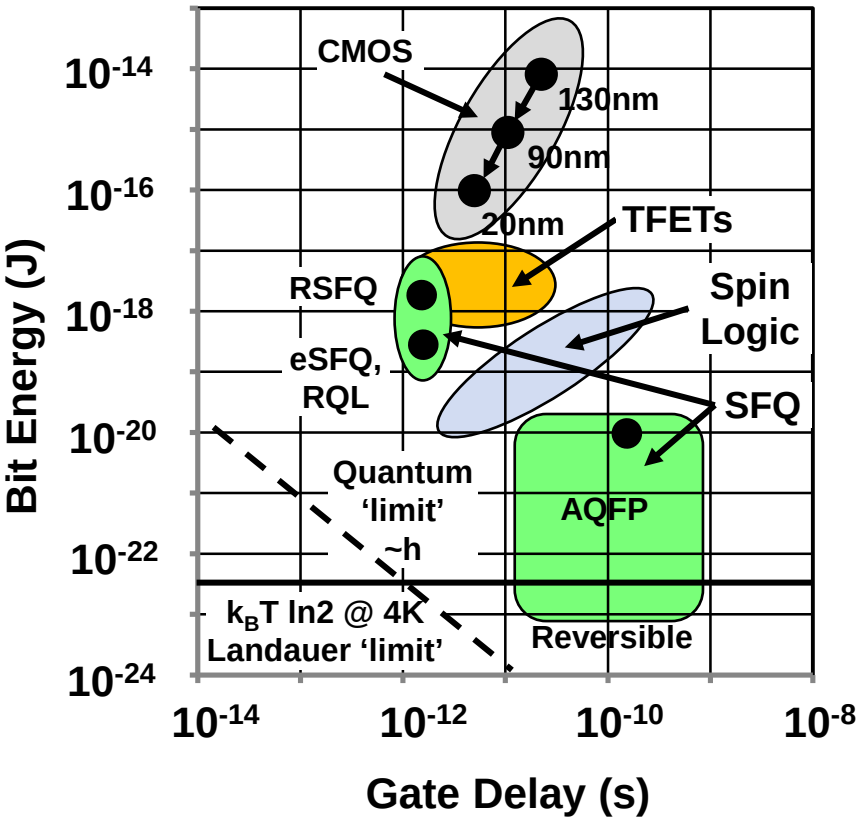
200-mm SFQ4ee Wafer



SFQ Circuit Technology is Immature

Superconducting electronics will not succeed if we view Josephson junctions as a drop-in replacement for CMOS transistors

- **Cold, hard facts**
  - As posed today, SFQ will not have the same density as CMOS circuits
  - Have not developed an optimal circuit design approach
  - Need an effective solution for data storage
- **Cold, hard facts (Part 2)**
  - SFQ information process is uniquely energy efficient
  - SFQ circuits can be designed for 10X higher clocks than CMOS
  - SFQ circuits have access to a quantized reference (fluxon)
    - Unique advantage for mixed-mode signal processing



Need to develop a computing paradigm that takes advantage of SFQ strengths

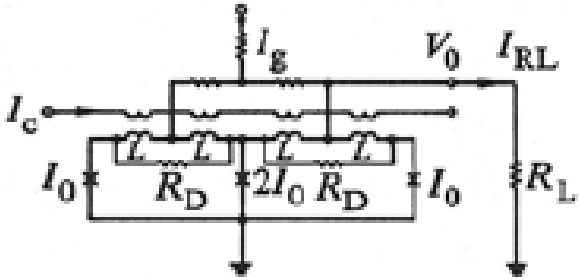
Outline

- Short history of SFQ fabrication and circuit develop
- State-of-the-art SFQ fabrication
- Scaling limitations and EDA needs
- Summary

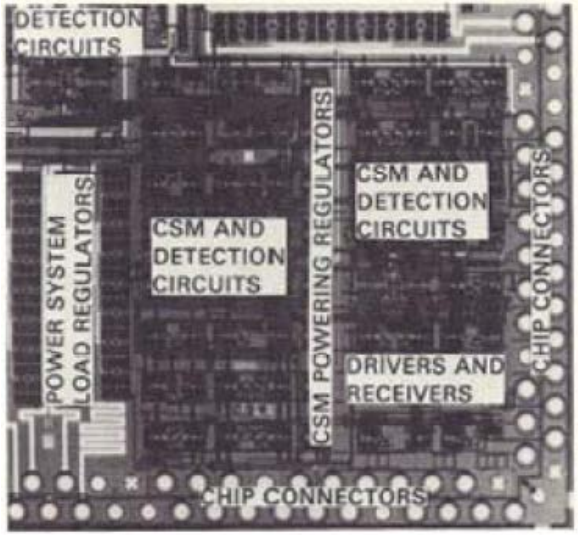
1st Gen SFQ: Latching Logic
IBM 1970's to early 1980's

- **Logic gate formed from interferometric circuits containing several Josephson junctions**
  - Typically "AND" and "OR" gates
  - Designed to latch a voltage state
  - Bipolar power supply served as clock and data reset
- **Fabrication evolved to Nb base electrode with Pb-In-Au counter electrode**
  - Junction formed on the edge of the Nb electrode
  - Minimum feature size was 2.5 μm
- **Cross Sectional Model (CSM) experiment**
  - 10 logic levels, chip-to-chip data flow
  - 300 MHz clock
- **Project halted in 1983**
  - No path to clocks > 1 GHz
  - No viable memory
  - Continued advance of Si circuits

Three junction Interferometric Logic Gate



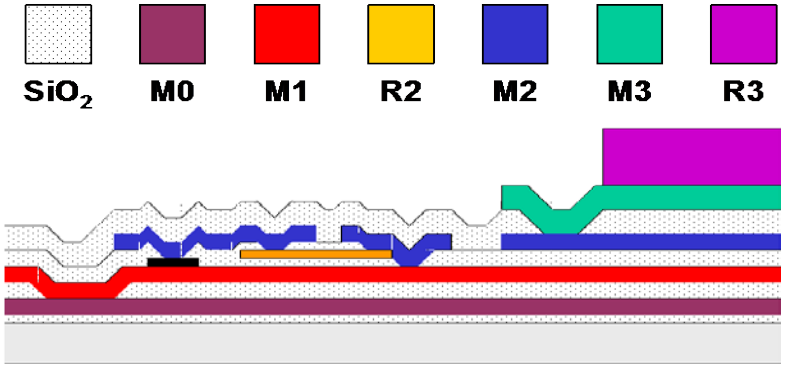
Portion of CSM Integrate Circuit



2nd Gen: Rapid Single Flux Quantum (RSFQ)
1990 – 2010's

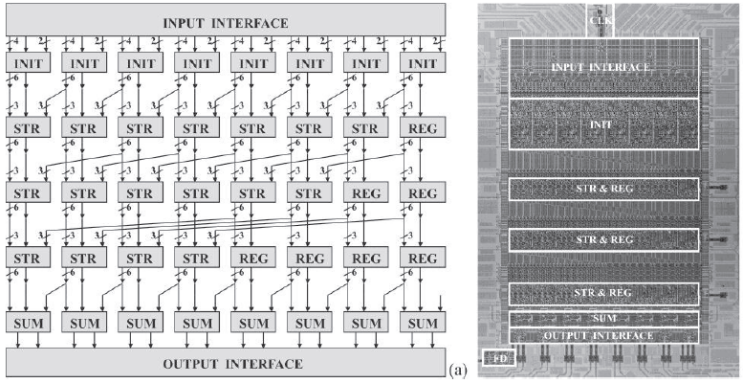
- **RSFQ design approach invented in 1985 at Moscow State University**
  - Several junctions per logic gate
  - Bits encoded in short voltage pulses
  - DC current bias
- **Fabrication based on Nb-Al-AlOx-Nb trilayer junctions**
  - Invented in 1971 at IBM
  - 4 Nb-layer standard process
  - Additional layers added in last decade
- **Many significant circuit demonstrations**
  - Single gate clock speed, 750 GHz
  - 8-32 bit adders, multipliers, ALU at clock speeds of 20 – 30 GHz
  - Analog-to-digital converters with sample rates >40 GHz
- **Circuits limited to ~20k JJs**

Hypres 4-Metal Layer Process



- 4 Nb wiring layers
- Feature size > 1μm
- Typical junction I_c 100μA, J_c 1 – 4.5 kA/cm^2

8-bit ALU with 20 GHz Clock



(Filippov, 2012)

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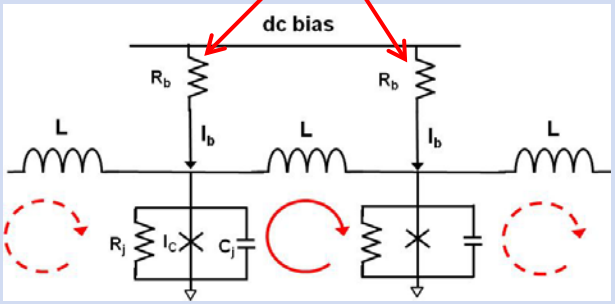
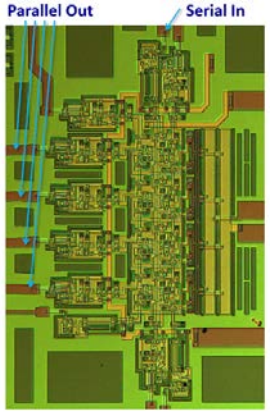
3rd Gen: No Bias Resistor Approaches
RQL, eRSFQ, eSFQ

Conventional RSFQ Biasing

Resistive biasing dominates power dissipation



eSFQ Circuit Design Approach (Hypres)

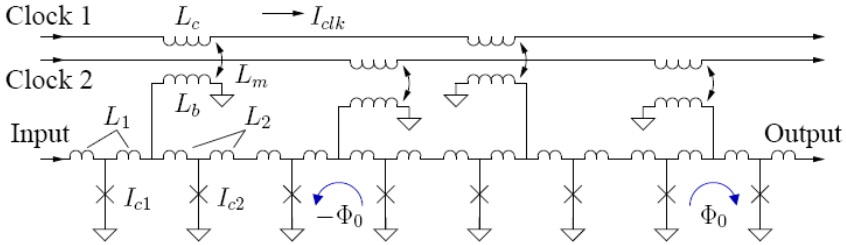


- Replace R in bias circuit with L
  - DC bias with minimal dissipation: in JJ shunt resistors only during switching
  - Can adapt standard RSFQ gates to eSFQ
- 0.8 aJ/bit eSFQ shift register and deserializer test circuits*

Reciprical Quantum Logic, RQL (Northrup Grumman)

- AC Clock, no dc bias resistor dissipation
- Inductively coupled to RF signal line to power devices / eliminates ground return
- Four-phase clock to provide directionality of the SFQ pulse propagation
- "1"s are encoded as a reciprocal pair of SFQ pulses

Schematic of RQL Shift Register Bit



- ~0.1 aJ/bit 8-bit Kogge-Stone RQL adder
- 6.2 GHz clock

*Hypres 4.5 kA/cm^2

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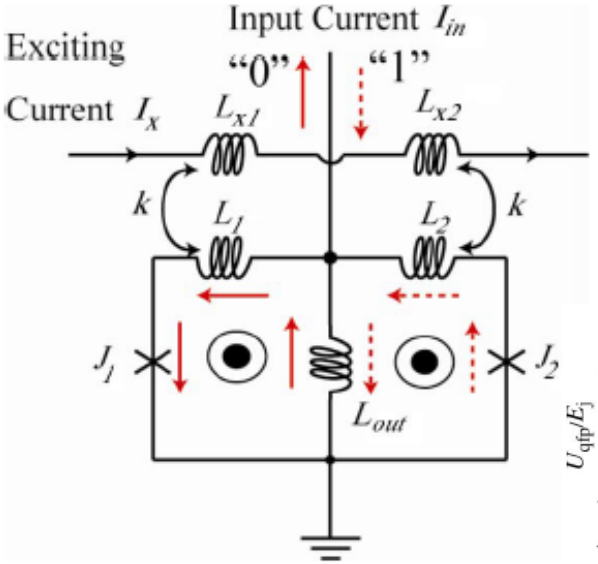
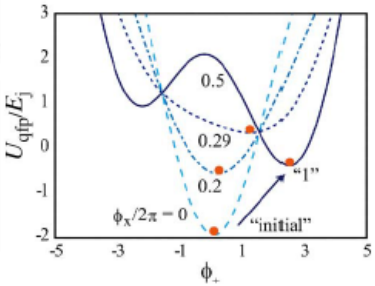
4th Gen: Adiabatic Quantum Flux Parametron (AQFP)

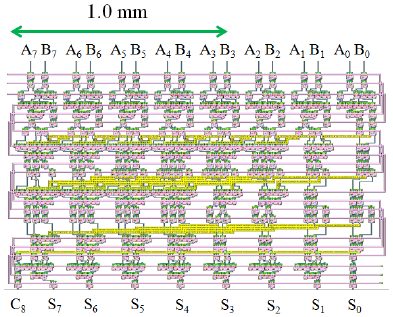
- **The bit is created with two connected loops, each with 1 JJ, inductively coupled to the control lines**
  - **Excitation current creates double-well potential**
  - **States '0' and '1' correspond to an SFQ stored on either side of circuit / double well potential**
- **In adiabatic operation, manipulate information without switching the JJs**
  - **'Gradual' rise/fall of excitation current for adiabatic operation**
  - **Switching energy << $I_C\Phi_O$, can be at Landauer limit**
  - **In constrast, 3rd gen SFQ switches JJs – energy per bit ~ $I_C\Phi_O$ = 1aJ**
- **Several recent demonstrations confirming the viability of the circuit design approach**
  - **Logic cells**
  - **Adder circuits with up to 20k JJs**





8-Bit Kogge-Stone Adder

Architecture	**Kogge-Stone**
Fab Process	**STP2 2.5 kA/cm²**
Number JJs	**1224**
Circuit area	**1.74 x 0.99 mm²**
Clock	**5 GHz**
Latency	**1400 ps**
Energy dissipation	**16.4 aJ for β_C = 1.0** **10.9 aJ for β_C = 5.0**



Takeuchi, 2013

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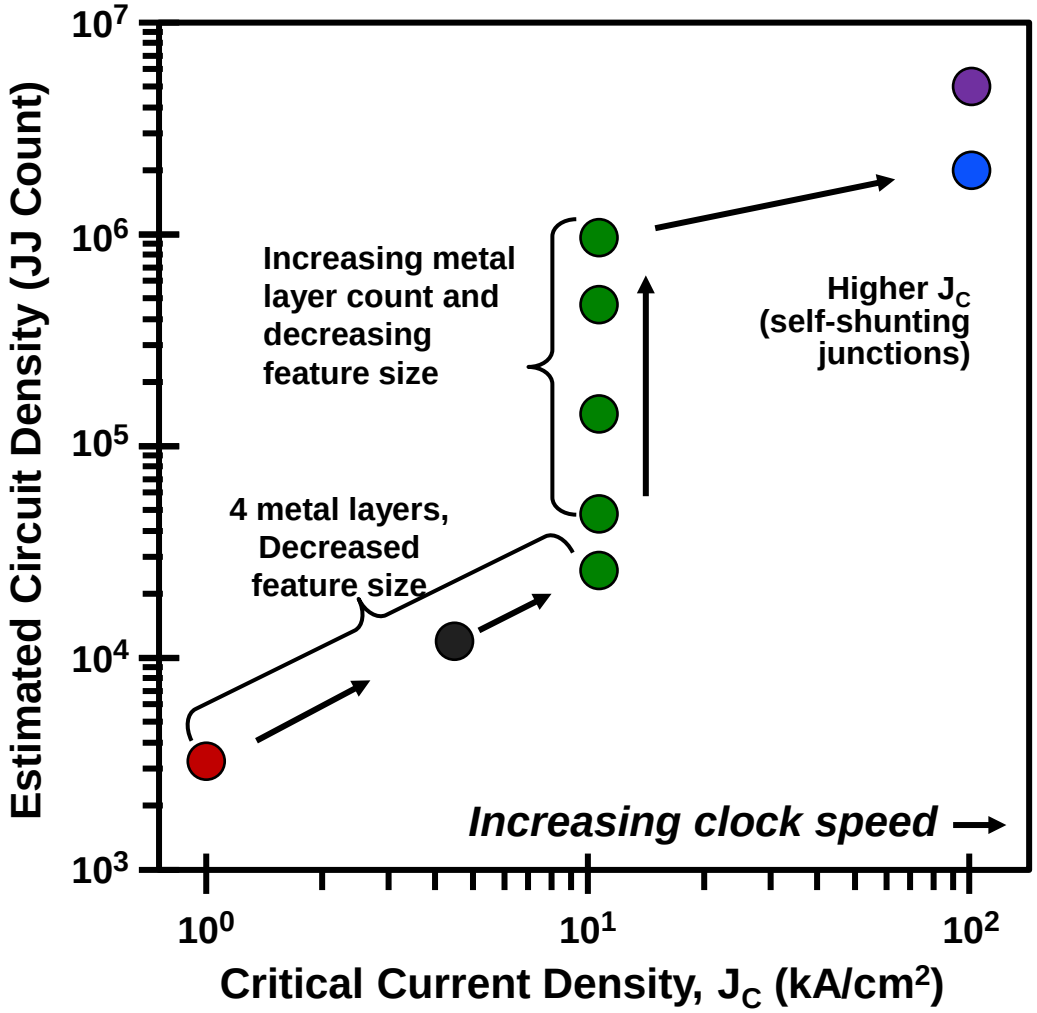
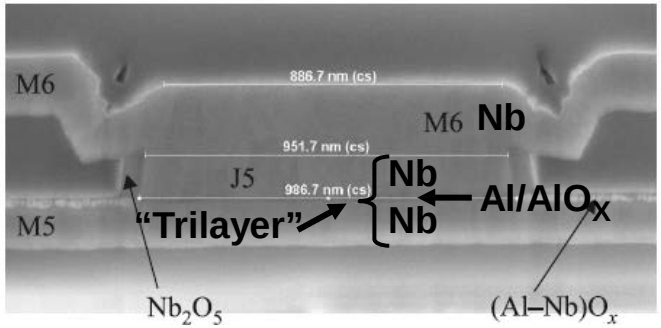
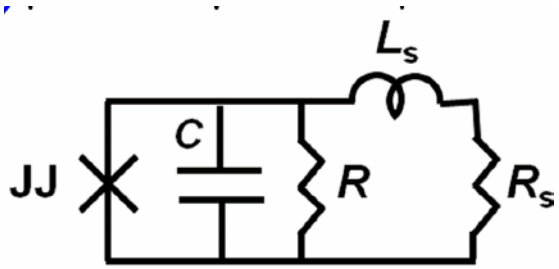
Strategy for Advancing SFQ Fabrication



Josephson Junction Cross Section



Resistively Shunted Junction



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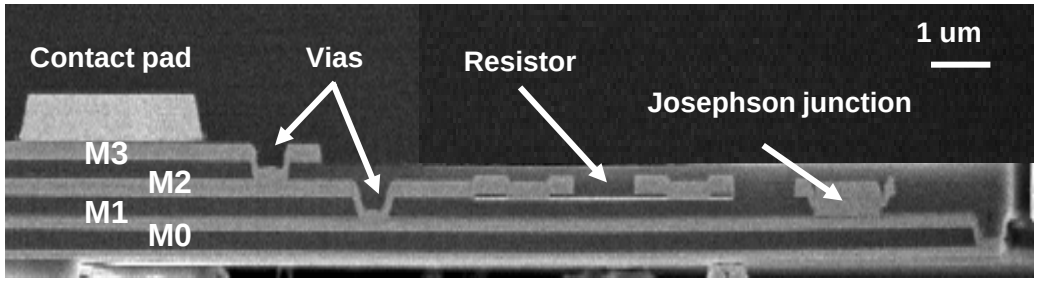
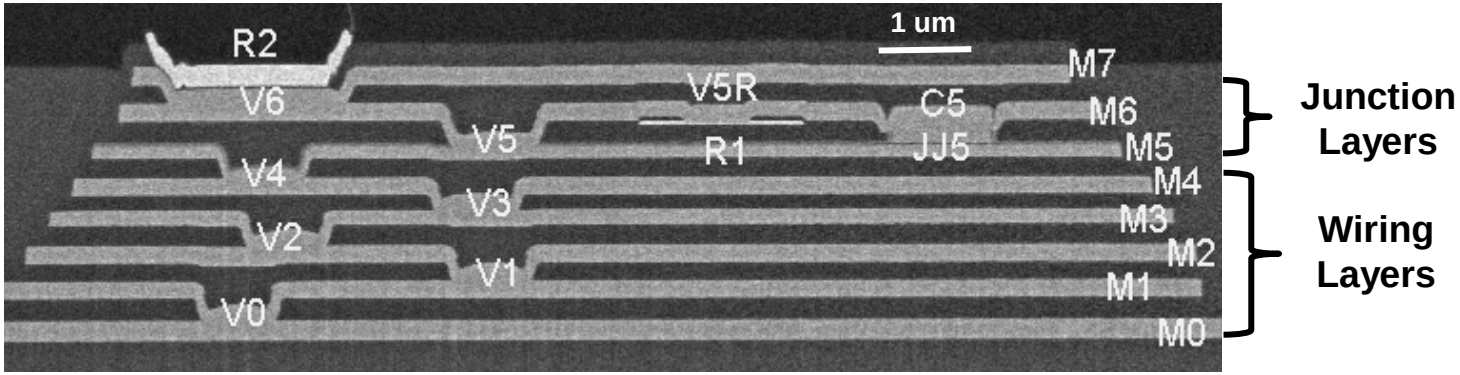
MIT-LL Process Progression

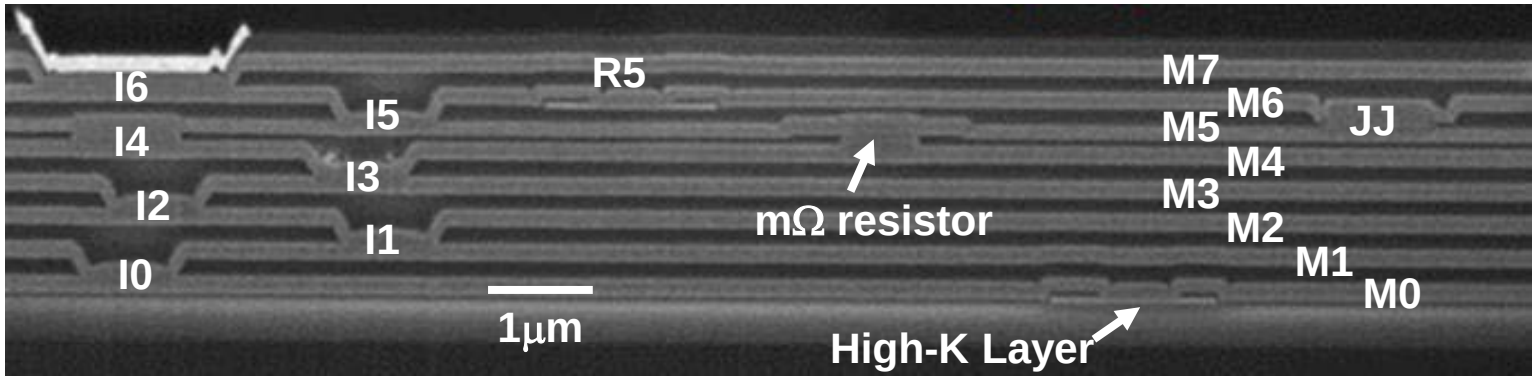
SFQ-3ee (4-Metal-Layer, 500nm min features)



SFQ-4ee (8-Metal-Layers, 500nm min features)



SFQ-5ee (8-Metal-Layers, 350nm min features)



Outline

- Short history of SFQ fabrication and circuit develop
- State-of-the-art SFQ fabrication
- Scaling limitations and EDA needs
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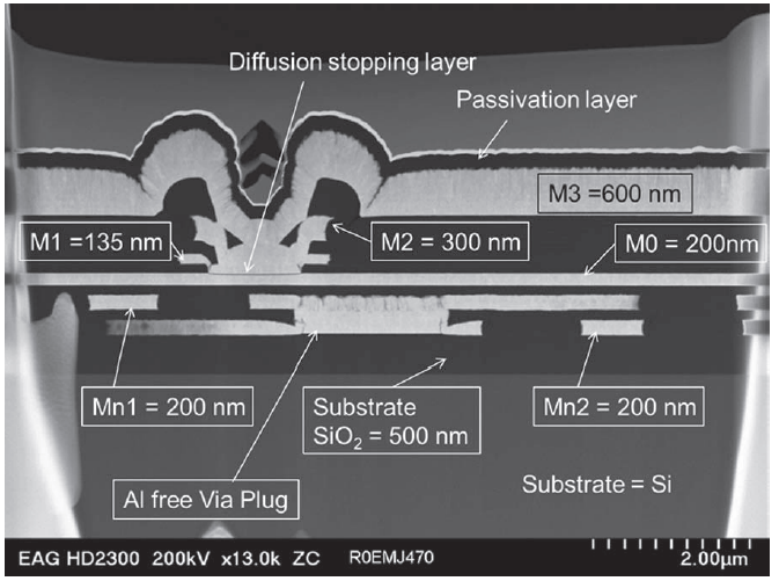
Hypres 6-Metal Layer Process (Ripple-2)

- **2 planarized layers beneath standard 4 metal layer process**
  - **0.1 kA/cm^2, 4.5 kA/cm^2 and 10 kA/cm^2 Jc processes available**
  - **Minimum wiring feature size**
    - **1 μm for 4-layer process**
    - **0.25 μm for 4+-layer process**
  - **Minimum junction size: 1 μm**
- **Working to add planarization to junction layers**

Ripple-2 Cross Section



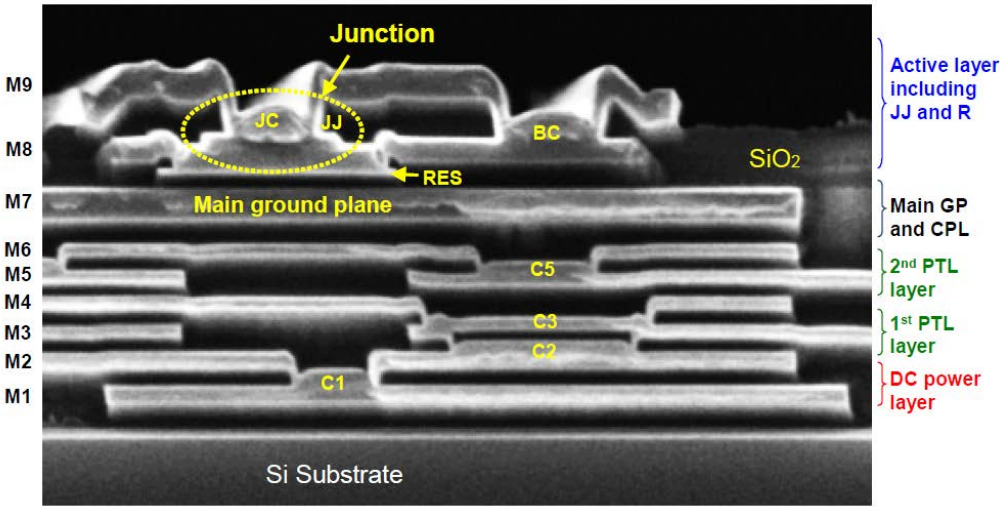
Hypres Fabrication Tools

- **150-mm wafers, significant refresh in 2012**
- **~2500 ft^2 of class 100/1000**
- **248nm stepper**
- **Planarization using "Caldera" process (etch + CM) for geometry independent planariation**

AIST-CRAVITY ADP2 9-Layer Process

- 9 Nb layers, M1-M7 planarized
- Additional CMP and thick metal under JJ layer
- 10kA/cm^2 and 20kA/cm^2 Jc processes
- Minimum feature size: 1μm
- Minimum junction size: 1μm
- Mo resistors with 2.6 Ω/sq
- Circuits demonstrated 69k JJ (shift register) and 19k JJ (logic)

AIST/Cravity ADP2 Process



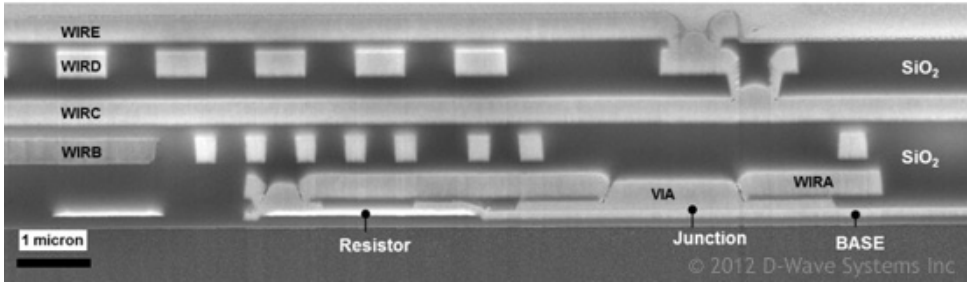
AIST/Cravity Fabrication Tools

- 75-mm wafer tool set
- 2900 ft^2, class 100 / 1000 cleanroom
- i-line stepper

D-Wave Systems 6-Metal Layer Process
Fabricated at Cypress

- **Fully planar 6-metal layer process**
- **Process Jc is 0.4kA/cm^2 (for qubits)**
- **Minimum feature size: 250nm**
- **Minimum junction size: ~500nm**
- **Circuits demonstrated with 125k JJs**

D-Wave 6-Nb-Layer Process



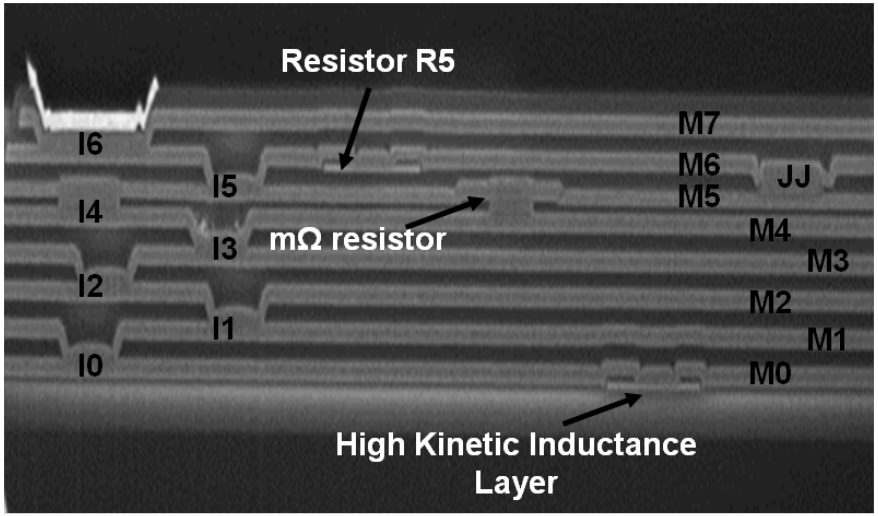
Cypress foundry in Bloomington, MN

- **200-mm production tool set**
- **80k ft^2 class 10 cleanroom**
- **90nm-350nm baseline flows in production**
- **Development access to production environment**
- **DMEA trusted foundry**
- **~ 400 employees**

MIT-LL 8 Metal Layer Process

- Fully planarized 4, 8, and 10 Nb wiring layers
- Minimum feature size 350 nm (248 nm lithography)
- Minimum junction size <500nm
- 10kA/cm^2, 20kA/cm^2 and 50kA/cm^2 (experimental) processes
- Demonstrated circuits with ~70k JJs (shift registers)

MIT-LL 8-Layer Nb Process



MIT-LL Fabrication Facility

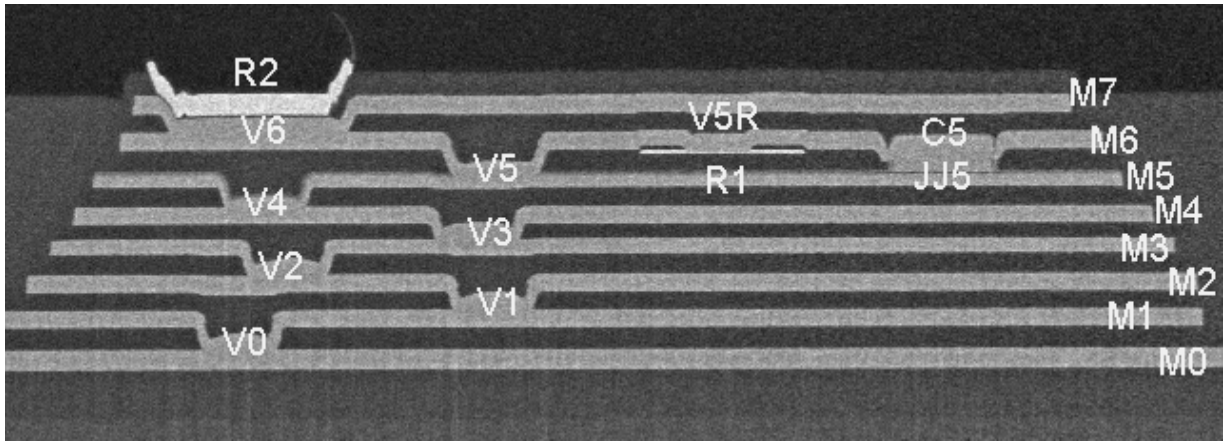
- 200-mm production tool set
- 8k ft^2 class 10 cleanroom
- 90nm baseline flows in prototype circuit quantities
- Multi-use facility: CMOS, Si imagers, Nb SFQ, GaN on Si, MEMS, microfluidics
- DMEA trusted foundry
- ~ 65 dedicated staff; 24/5 operation

IARPA SFQ Technology Roadmap
(*Government Foundry, MIT-LL*)

Fabrication Process Attribute		Units	Process Node					
			SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ7ee	SFQ8ee
Critical current density		MA/m^2	100	100	100	100	100	100
JJ diameter (surround)		nm	700 (500)	700 (500)	700 (300)	700 (300)	500 (200)	500 (200)
Nb metal layers		-	4	8	8	10	10	10
Line width (space)	Critical layers	nm	500 (1000)	500 (700)	350 (500)	350 (500)	250 (300)	180 (220)
	Other layers	nm			500 (700)	500 (700)	350 (500)	250 (300)
Metal thickness		nm	200	200	200	200	200	150
Dielectric thickness		nm	200	200	200	200	200	180
Resistor width (space)		nm	1000 (2000)	500 (700)	500 (700)	500 (700)	500 (500)	350 (350)
Shunt resistor value		Ω/sq	2	2	2 or 6	2 or 6	2 or 6	2 or 6
mΩ resistor		mΩ	-	-	3 - 10	3 - 10	3 - 10	3 - 10
High kinetic inductance layer		pH/sq	-	-	8	8	8	8
Via diameter (surround)		nm	700 (500)	700 (500)	500 (350)	500 (350)	350 (250)	350 (200)
Via type, stacking		-	Etched, Staggered	Etched, Stacked \2/	Etched, Stacked \2/	Etched, Stacked \2/	Stud/Plug, Stacked	Stud/Plug, Stacked
Early access availability		-		2014	2015	2016	2016	2017

Drives increased density Recently added

MIT-LL SFQ4ee Process



Junction Layers

Wiring Layers

Process Features

- Wafer size: 200 mm
- JJ technology: Nb/Al-AlO_x/Nb
- J_c: 10 kA/cm^2 (100 μA/μm^2) baseline
- Number of Nb layers: 8
- Min JJ size: 700 nm
- Min wiring size: 500 nm
- Min spacing: 700 nm
- Full planarization of all layers by CMP
- Fab cycle time: <2.5 months, 8 wafers

Integration Scale Demonstrated

- AC-biased SFQ shift registers with 32.8k JJs (Semenov, 2015)
- RQL shift registers with 32.8k and 40k JJs on a chip (Herr, 2015)
- AC-biased SFQ shift registers with 65,000+ JJs per circuit (Semenov, SBU)
- AC-biased SFQ shift registers with 144,000+ JJs - under test (Semenov, SBU)

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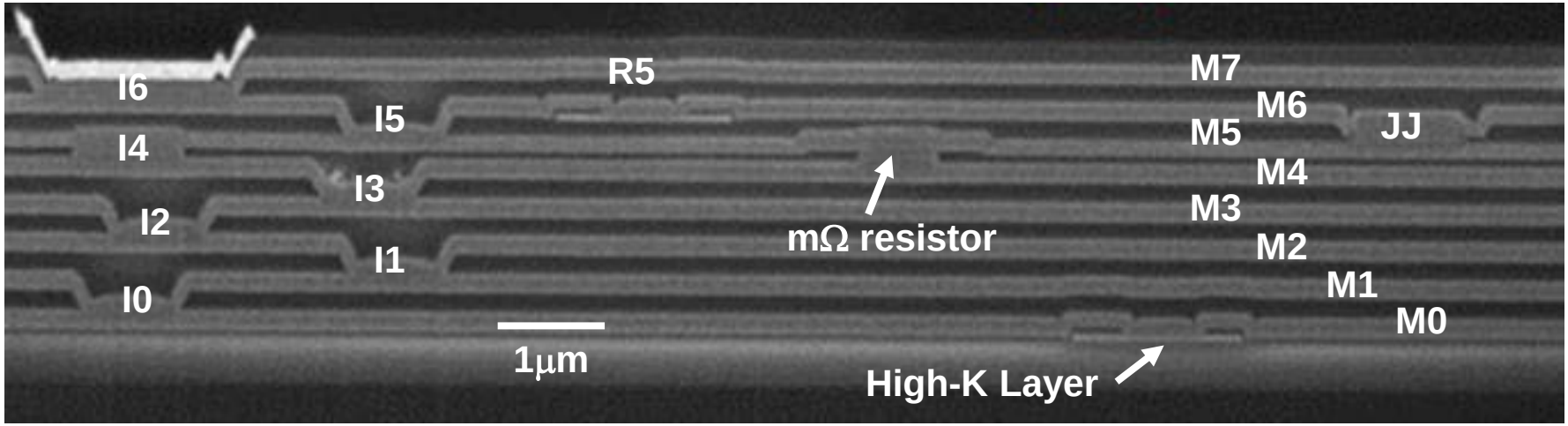
SFQ5ee Process and Features to Increase Circuit Density

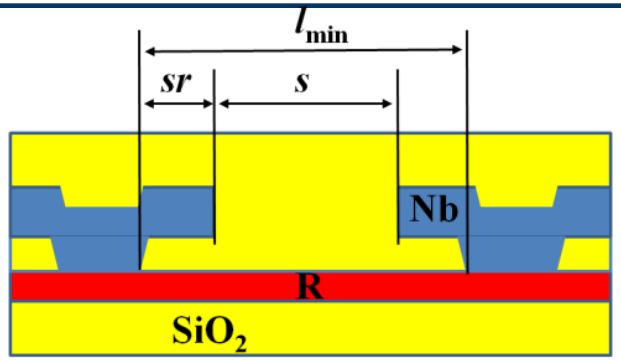


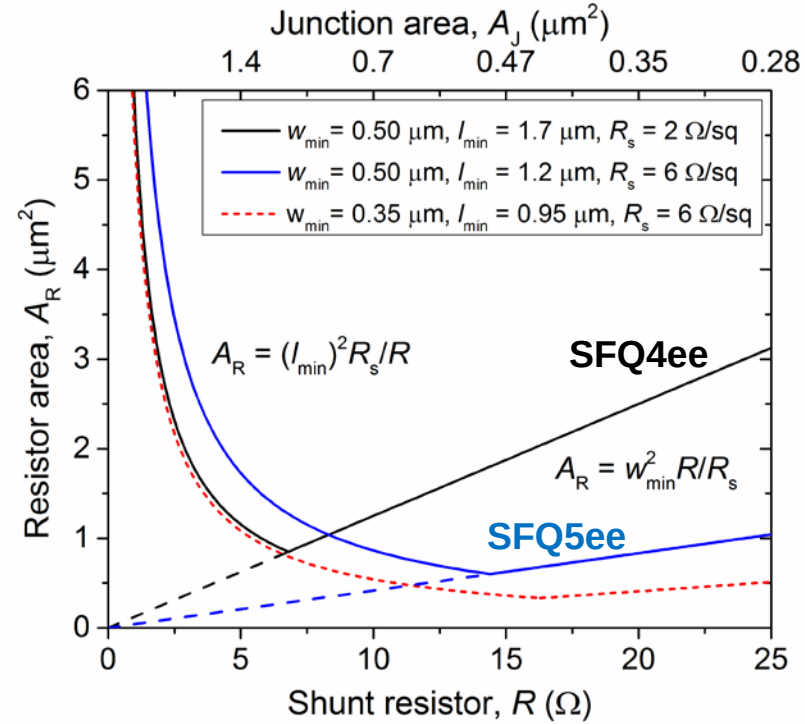
Enhancements over SFQ4ee:

- **Min linewidth and spacing: 0.35 μm except M0, M1, and R5 (0.5 μm)**
- **Min size of vias and metal surround: 0.5 μm and 0.35 μm, respectively**
- **2 Ω/sq (Mo) or 6 Ω/sq (MoN_x) resistors for JJ shunting and biasing**
- **High kinetic inductance to enable compact bias inductors for ERSFQ**
- **mΩ resistor between Nb layers M4 and M5**

More Deeply Scaled Resistors
MoN_X Resistors

- **Issue: shunt resistors occupy a considerably larger area than JJs**
- **In SFQ4ee, resistors made from Mo**
  - w = 0.5 µm, R_s = 2 Ω/sq, $2A_{via}$ ~ 1 µm^2
  - RQL circuits use JJs with I_c ~35µA → R ~ 20 Ω, and
    A_r ~ 5 µm^2 >> A_J - JJ area
- **In SFQ5ee, option for MoN resistors**
  - R_s = 6 Ω/sq, ℓ_{min} = 1.2 µm
  - R = 20 Ω, ~ 1µm2
  - T_c < 2 K
  - Wafer 1σ = 2.3% on patterned resistors





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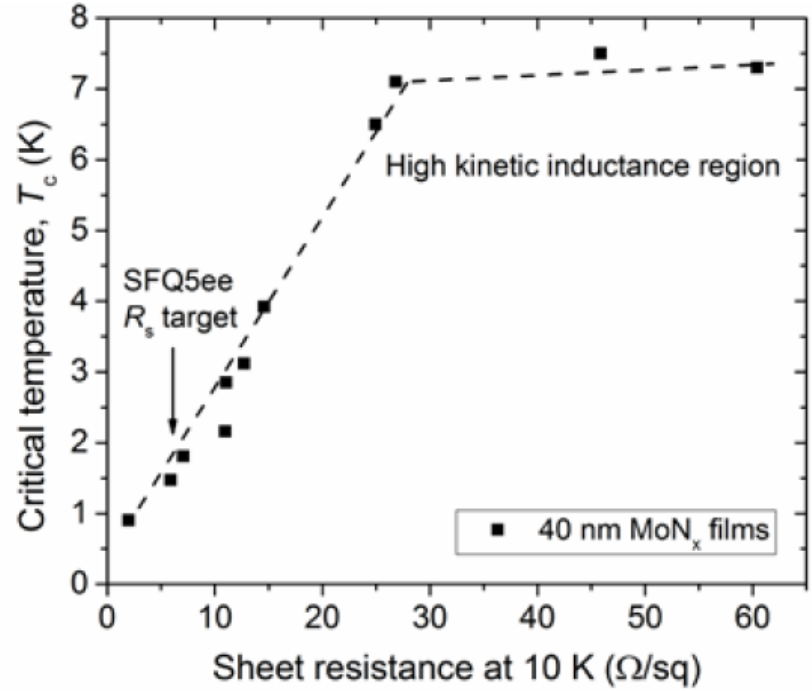
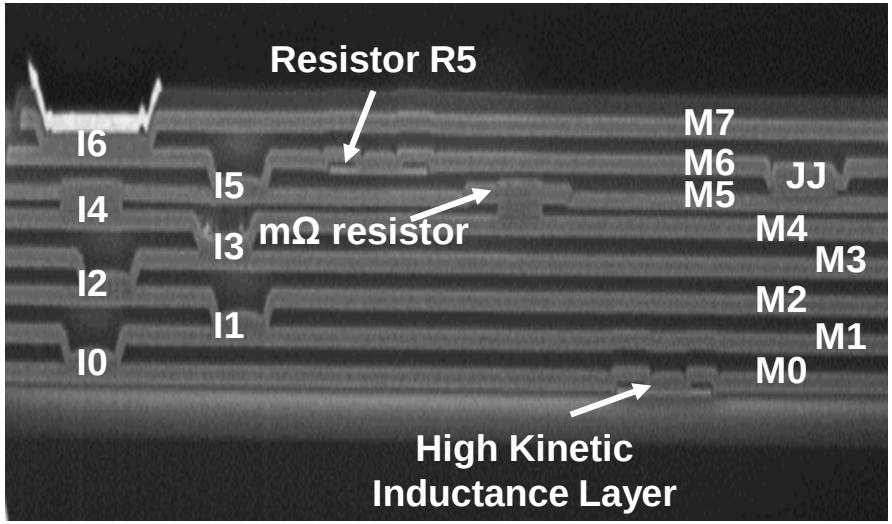
More Deeply Scaled Bias Circuitry
MoN_X High-Kinetic-Inductance Layer

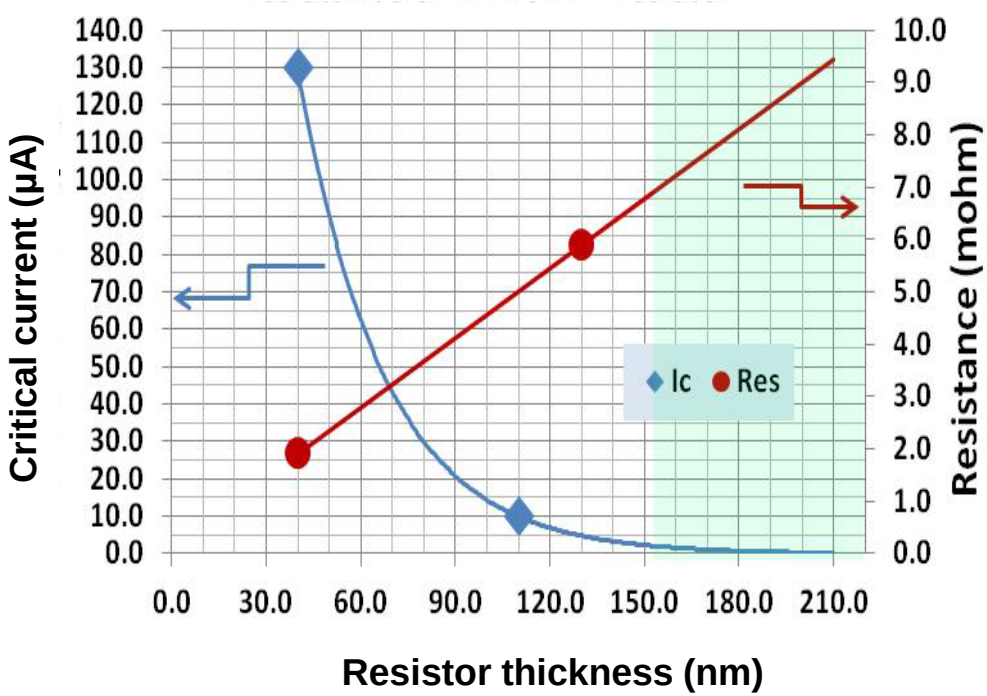
- **Issue: Energy-efficient RSFQ requires multiple 100-pH bias inductors**
  - **Conventional (geometric) inductor occupies typically ~ 100 μm² area, L_g < 1 pH/sq**
- **Kinetic inductance L_k of thin superconducting films >> geometric inductance:**
  - **Need film thickness, d , to be much thinner than penetration depth, λ**
- **For practicality: *d* ~ 35 nm - 40 nm, so λ needs to be ~ 400 nm – 500 nm,**
  - **MoNX with higher nitrogen content is an effective choice**
  - **Area savings: at L_k = 10 pH/sq and *w* = 0.7 μm, $A_k \sim A_g/20$**

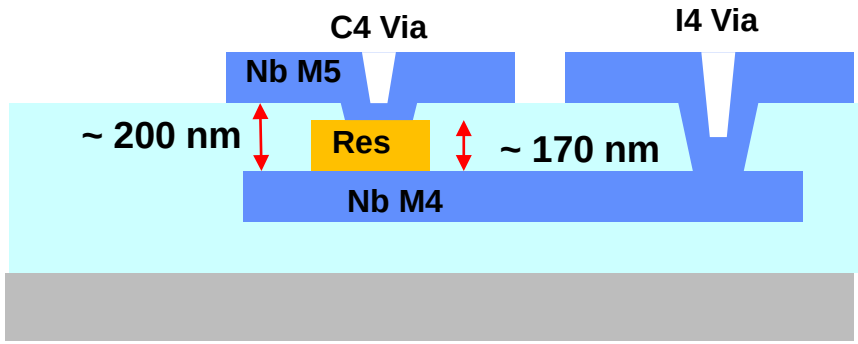




Flux Trapping in More Deeply Scaled Circuits
mΩ-range Resistors

- **Issue: SFQ circuits are sensitive to flux trapping: external and internal**
  - **With circuit density increasing, flux trapping could increase**
    - **Diminishing distance between flux-trapping moats and inductors**
    - **Diminishing size of the moats**
  - **Some SFQ cells are particularly sensitive, cannot be reset**
- **Possible remedies:**
  - **Break some of the superconducting loops by mΩ-range resistors**
  - **Improved circuit and moat design**
- **Fab solution: add extra resistive layer**
  - **Resistor thickness required to be in the 'green' area is between 150 nm and 180 nm**
  - **Pursuing Mo and MoN_X resistors**

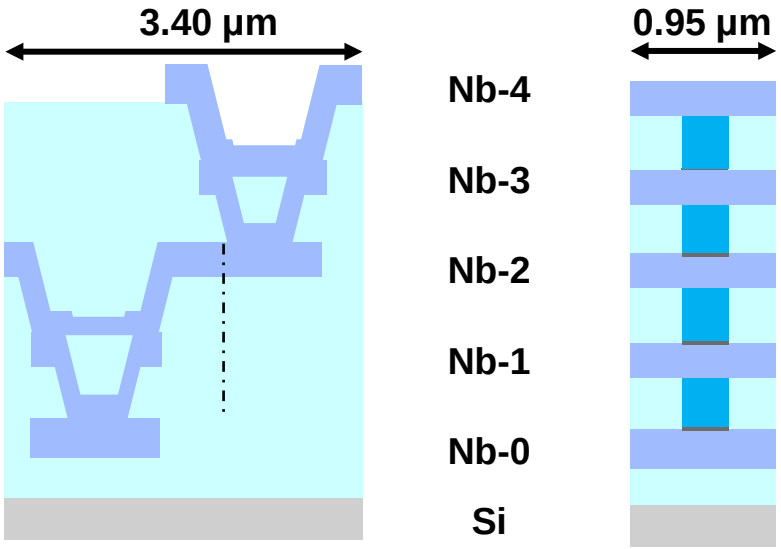




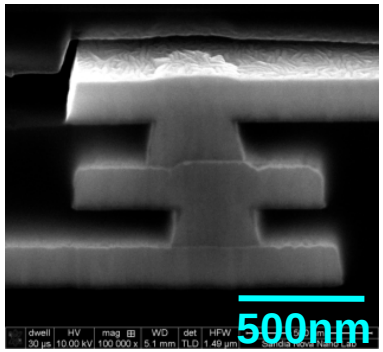
Higher Density Vias: Etched vs Stacked

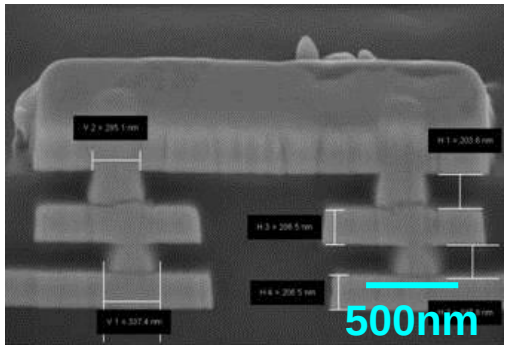
- Stacked vias permit
  - Decrease in size
  - Increase in performance
- Have developed a stud via process that can be stacked
  - Nb-Al-Nb trilayer (without oxide)
  - Diameters down to 250nm
- Significant increase in complexity of the fabrication
  - 2X increase in metal dep, photo masks, CMP time (30% increase in number of steps)
  - Complicates CMP: more stringent density requirements, requires higher uniformity
- In parallel, pursuing a damascene, CVD process for plug or plug+line formation

Etched, Staggered Via | **Stacked Via**



360nm Stud Via Test Structure

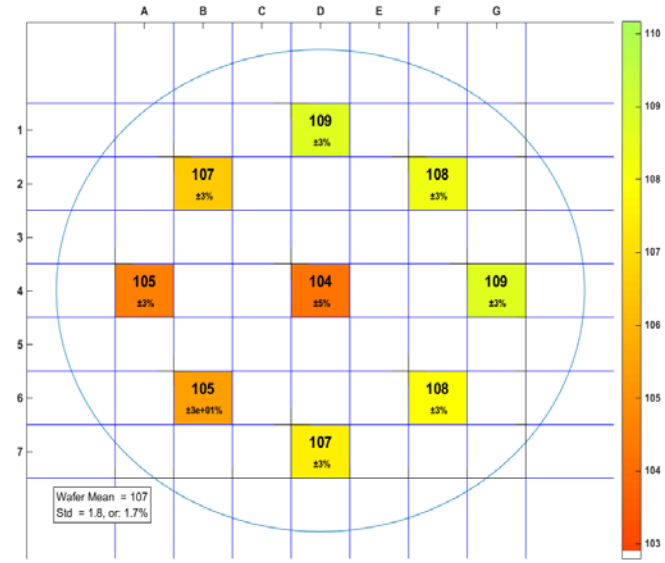




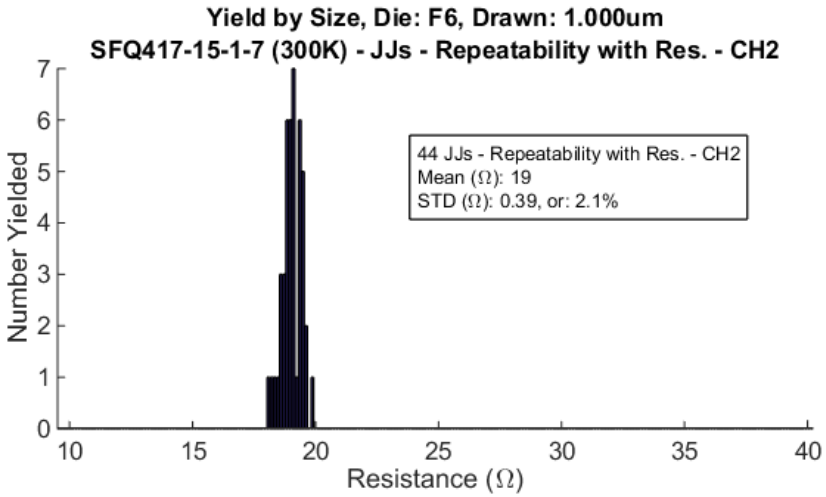
Process Control Monitor (PCM) Test Data

- **PCM reticle included on all SFQ wafers**
  - **3255 test structures on 16 chips**
  - **9 “drop-out” reticle shots per wafer**
- **Complete room temperature testing**
  - **Junction Jc’s, ‘spreads’ and topography effects**
  - **Via strings**
  - **Snakes and combs on wiring layers**
  - **Resistors**
- **Selected cold temperature testing**
  - **Junction Jc**
  - **Inductor structures**
  - **Line and via critical current**
- **Extensive software**
  - **Automated measurement**
  - **Calculating parameters of interest**
  - **Assessing process splits and historic comparisons**

Critical Current, J_C Wafer Map



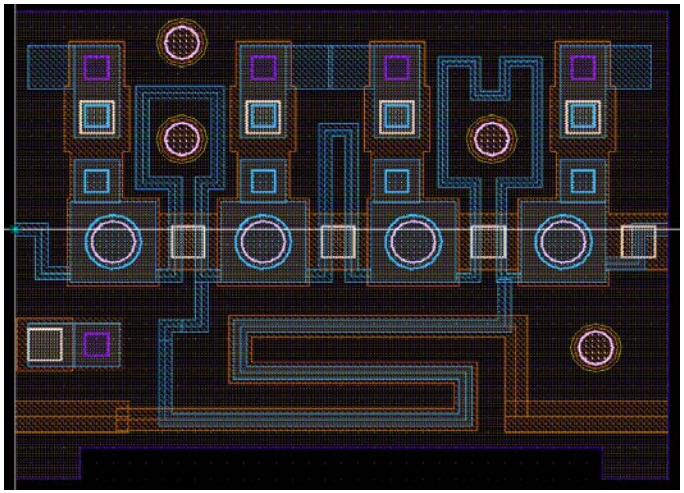
JJ Room Temp Resistance Histograms



Advanced Process Test Vehicle
Flux Shuttle Shift Register

- **Best to test actual digital circuits**
  - **Need a digital circuit scalable to ~1M JJs**
  - **Measure margins of individual cells, identify defects and trapped flux**
- **Employed a very old (before SFQ) idea: ac-biased, inhomogeneous" flux shuttle***
  - **4 JJs per bit**
  - **Stony Brook U design (V. Semenov)**
- **Results**
  - **Can observe trapped flux and operation at cell level**
  - **Cell operation variation: $1\sigma = 1\%$**
  - **Exceptional uniformity of Josephson junctions, $1\sigma_{JJ} = 0.8\%$**

4th Gen Flux Shuttle Layout (15x10μm)



Gen	#Bits	#JJs	Min Line (μm)	Cell Size (μm²)	JJ Density (per cm²)	Status
1st	8k	33k	0.5	40x17	0.6M	Func
2nd	16.4k	66k	0.4	20x15	1.3M	Func
3rd	36k	144k	0.4	20x15	1.3M	Test
4th	80.2k	321k	0.4	15x10	2.7M	Fab

* G.M. Lapir, (1977)

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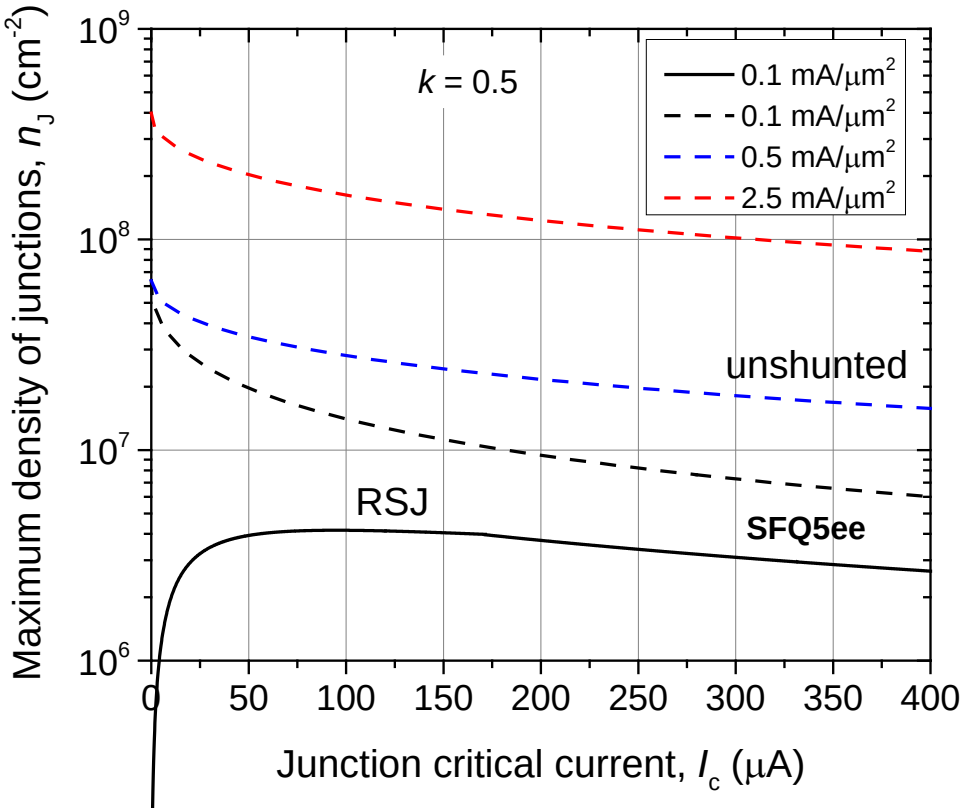
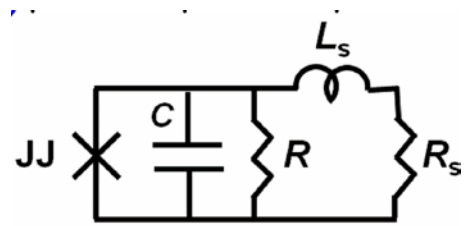
Outline

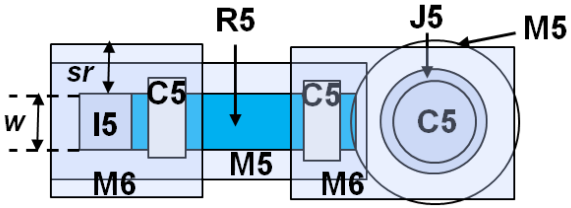
- Short history of SFQ fabrication and circuit develop
- State-of-the-art SFQ fabrication
- Scaling limitations and EDA needs
- Summary

Circuit Density Based on Josephson Junction Limitations





Resistively Shunted Junction



- $n_J = kIA_J$, fill factor k = 0.5
- Max density limited by the area of RSJ (~ 12 μm^2 per RSJ)
- 10x increase if get rid of shunts ⇨ self-shunted JJs

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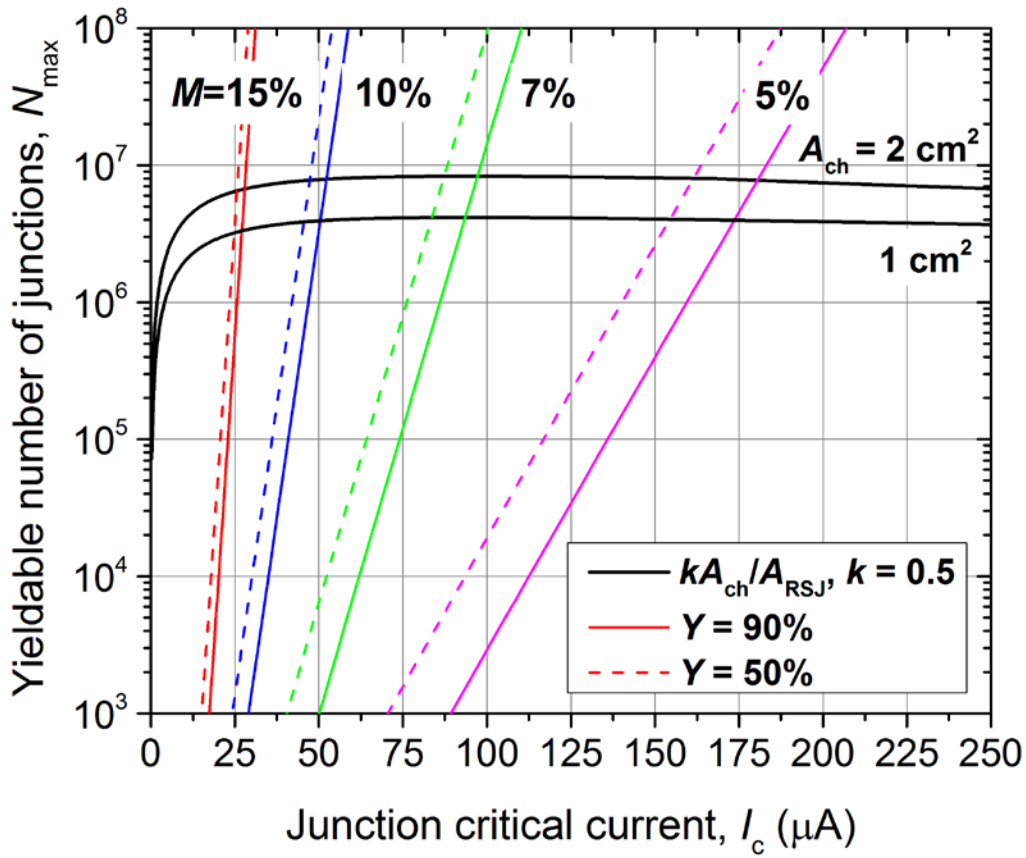
Maximum Circuit Size (#JJs) Based on Parametric Yield Limitations

- **Circuit yield is determined by**
  - **Operating margins designed into the circuit**
  - **Variation of the Ic's in the JJs (Lower Ic's have larger variations)**
- **Intersection of lines show minimum Ic needed as a function of # JJs and design margin**



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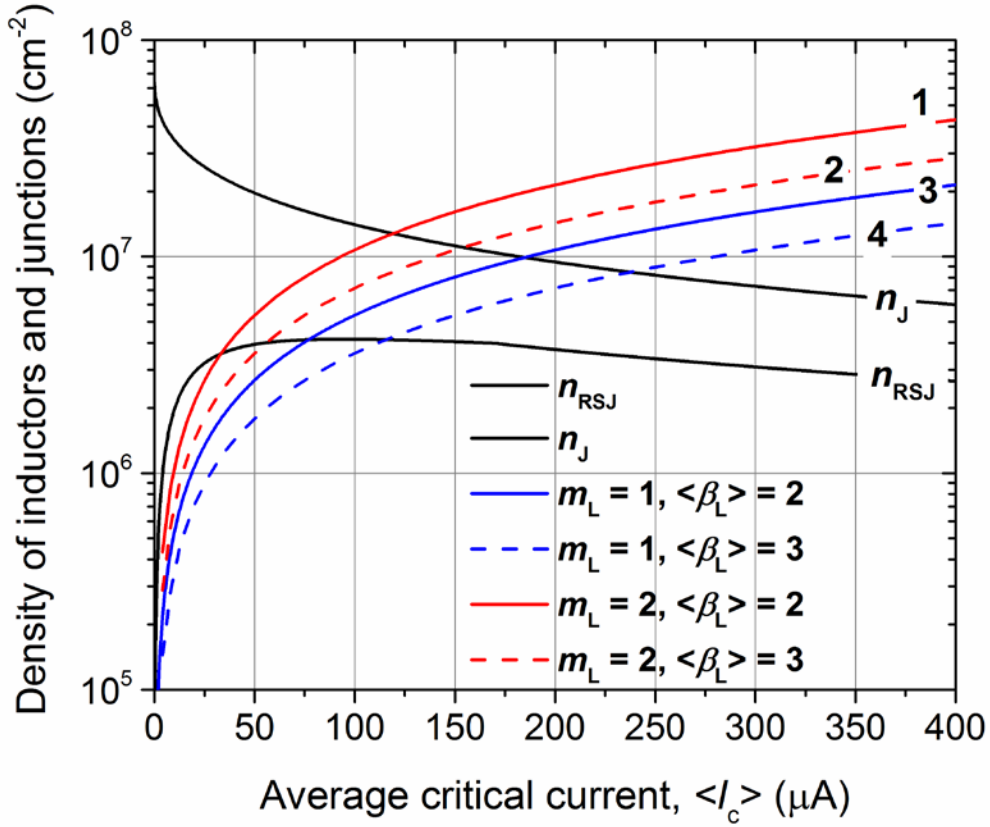
Circuit Density Based on Inductor Limitations

- **Circuit density is also limited by inductors**
  - **Each JJ requires an inductor, value is dependent on Ic of JJ**
- **Red and blue curves show potential inductor density as a function of**
  - **Inductors on 1 or 2 layers**
  - **Damping parameter of JJ**
- **Need to choose Ic greater than intersection of the inductor and JJ density curves**



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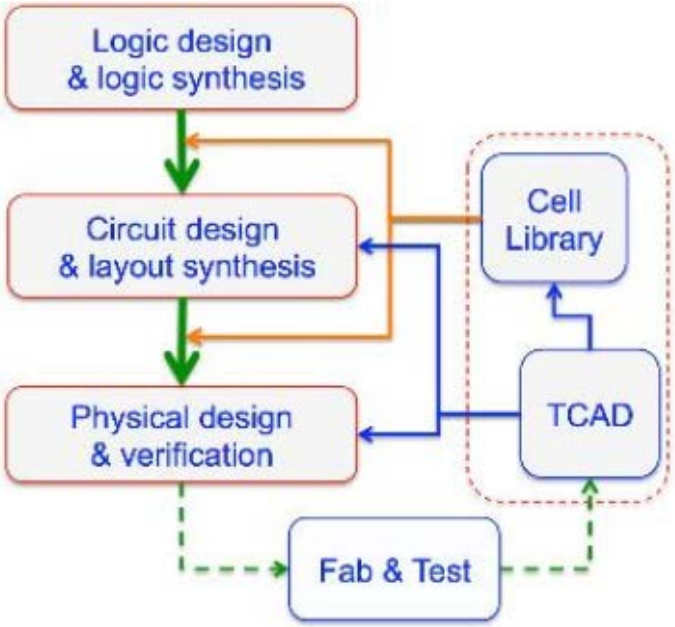
Design Tool Limitations for SFQ Circuits

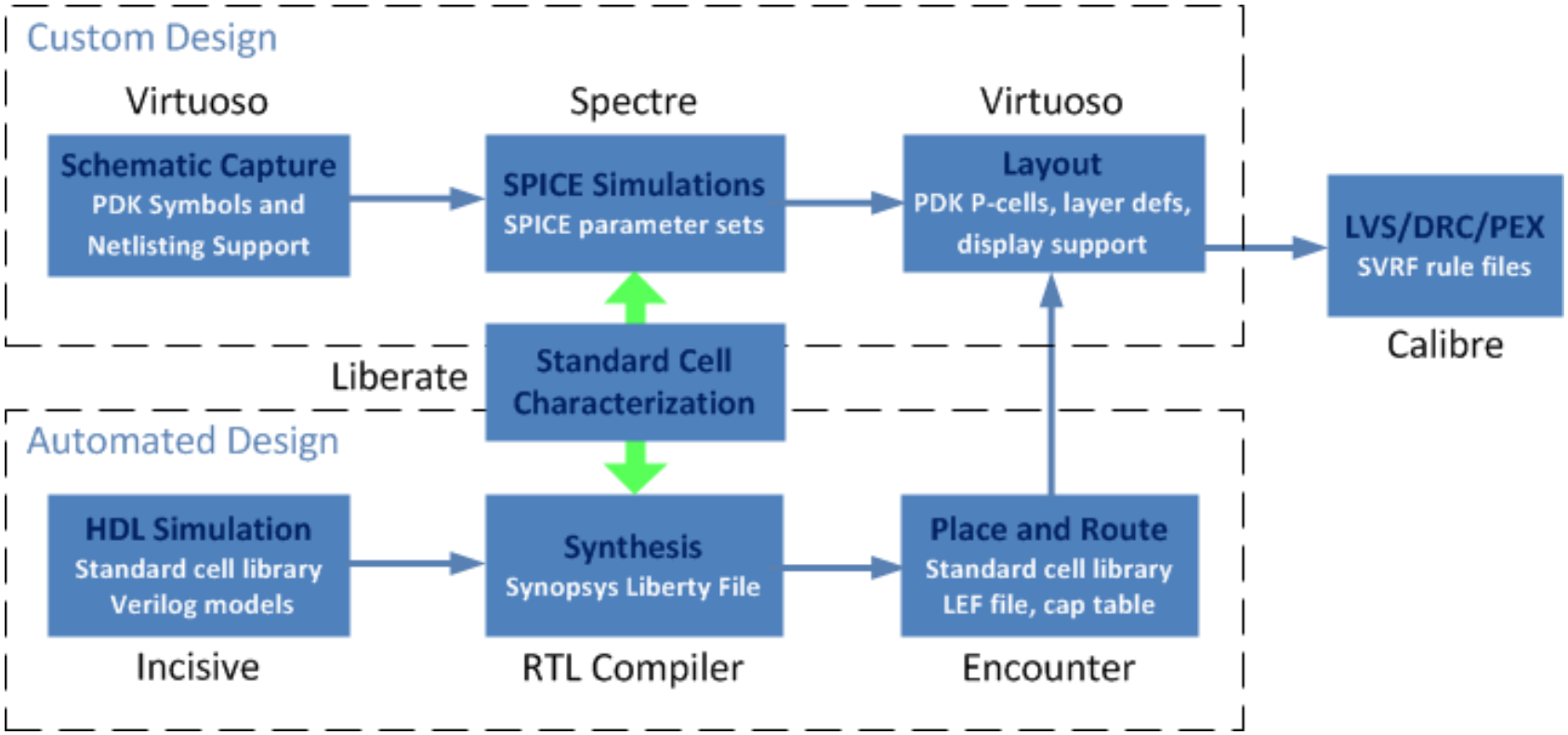
Electronic design automation (EDA) tools needed at all levels of SFQ design

- **Technology CAD (TCAD)**
  - Junction barrier design
  - Fabrication impact on component performance and tolerance
- **Custom design flows: I-V based circuit simulation**
  - Compact models of Josephson junctions and other components
  - Simulator for circuits with 100s of JJs (J-Spice)
  - Analog circuit design
- **Standard-cell design flow: HDL based design**
  - Standard cells based on different design approaches
  - Timing and data synchronization
- **Physical verification**
  - Layout versus schematic (LVS)
  - Magnetic design rules (flux trapping mitigation)

Standard Cell Design Flow
(from SuperTools Proposer's Day)

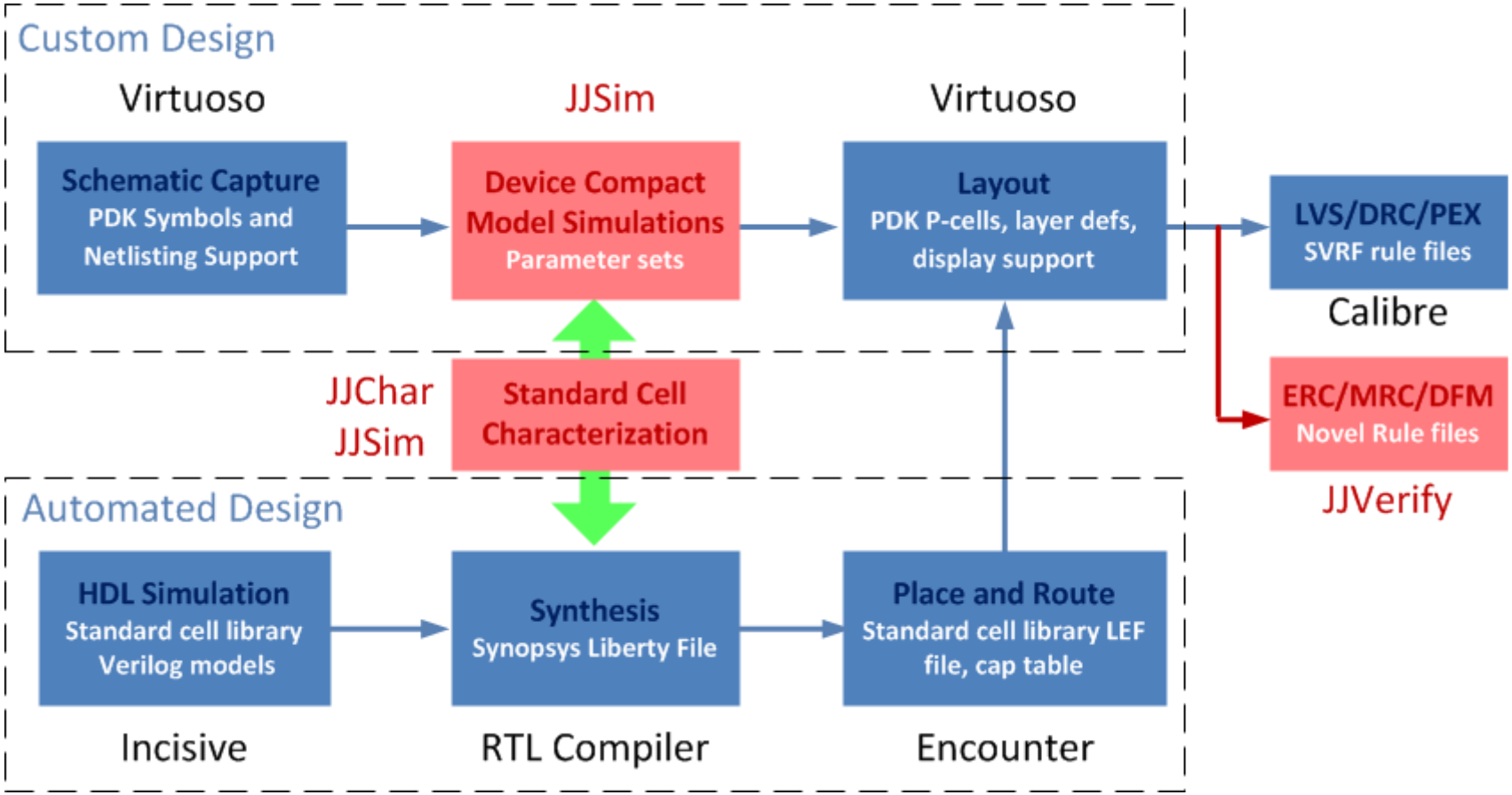


MIT-LL CMOS Validated Design Flow



- **Example EDA flow that supports custom and standard cell designs**

SFQ Circuit Hypothetical Design Flow



- **Modules requiring substantial modification are highlighted in red**
- **Maintain modularity and interface approaches common in CMOS EDA**

Outline

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SFQ Fab is as Cheap as Dumbed-Down CMOS

- **Current IARPA programs to mature SFQ design and fabrication are vital to the continued maturation of the technology**
- **IARPA C3 SFQ roadmap**
  - **On track to develop circuits with JJ density > 1M/cm^2**
  - **On track to demonstrate circuits with > 1 MM JJs-**
  - **100X increase over state-of-the-art at program start**
- **With 3rd generation energy-efficient design techniques, limits to the circuit density of < 10M JJs/cm^2**
  - **SFQ fab could be as cheep as dumbed-down Si processing**
  - **Can use multi-chip module approaches for near and mid-term demonstrations**

SFQ Circuit Technology is Immature: Needs Continual Assessment of Goals

- **SFQ has unique attributes that make it relevant for beyond CMOS applications**
  - **Potential for Landauer limit operation**
  - **Potential for > 50 GHz clock speed**
  - **Built-in quantized resources for mixed-signal applications**
- **Still relatively immature**
  - **Impressive demonstrations that validate potential of the technology**
  - **IARPA C3 program can solidify viability of the technology**
  - **Further investments needed for**
    - **Develop 'industrial scale' EDA tools**
    - **Maturation of fabrication and testing infrastructure**
- **Potential paths beyond the C3 horizon**
  - **Maturation of adiabatic quantum flux parametron**
  - **Design approaches that are more tolerant of fabrication variations**
  - **Novel device and circuit approaches for more deeply scaled nodes**