Lessons from an Emerging Technology: Superconducting Computing

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Future Supercomputing Vision

- Hybrid technologies: digital (CMOS, SFQ), probabilistic, analog, neuromorphic, reversible, and quantum computing (QC) — whatever works best!
- SFQ digital platform supports multiple cryogenic technologies
- Requires optical interconnects between room temperature and cryogenic nodes

Courtesy of the Oak Ridge National Laboratory, U.S. Department of Energy
Superconducting Computing Approach

- Low temperature operation (~4 K)
  - Allows different physics
  - Commercially available refrigeration

- Logic
  - SFQ (Single Flux Quantum)
  - Switching energy ~ 2x10^{-20} J

- Memory
  - compatible with SFQ logic

- Interconnects
  - Superconducting in the cold space
  - Input/Output: electrical or optical

- Major energy reductions in all 3 areas!
Notional Prototype, IARPA C3 Program

<table>
<thead>
<tr>
<th>Metric</th>
<th>Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock rate for superconducting logic</td>
<td>10 GHz</td>
</tr>
<tr>
<td>Throughput (bit-op/s)</td>
<td>$10^{13}$</td>
</tr>
<tr>
<td>Efficiency @ 4 K (bit-op/J)</td>
<td>$10^{15}$</td>
</tr>
<tr>
<td>CPU count</td>
<td>1</td>
</tr>
<tr>
<td>Word size (bit)</td>
<td>64</td>
</tr>
<tr>
<td>Parallel Accelerator count</td>
<td>2</td>
</tr>
<tr>
<td>Main Memory (B)</td>
<td>$2^{28}$</td>
</tr>
<tr>
<td>Input/Output (bit/s)</td>
<td>$10^9$</td>
</tr>
</tbody>
</table>

www.iarpa.gov/index.php/research-programs/c3
Status of Superconductor Electronics

Presented in this workshop:

- **IARPA Programs for Superconducting Computing**
  Marc Manheimer, IARPA

- **Energy efficient, high bandwidth digital data links between 4 and 300 K**
  Dr. Deborah Van Vechten, ONR
Digital-RF Receiver (Hypres)

- Commercial product with applications in:
  - Software-defined radio, satellite communications
- Directly digitizes RF (no analog down-conversion)
  - Ultra-wide bandwidth, multi-band, multi-carrier
- Hybrid temperature heterogeneous technology
  - Different technologies between ambient and 4 K
  - Closed-cycle cryogenic refrigerator

Quantum Annealing (D-Wave Systems)

- D-Wave® TwoX™ (2015 August 20), a commercial superconducting quantum annealing processor
- 128,000 Josephson junctions
- 1000 qubit array
- 15-20 mK operating temperature

“Washington” chip

D-Wave® TwoX™ quantum annealing processor
Electronics Technology Roadmaps

- **1993-1997** **NTRS**: National Technology Roadmap for Semiconductors
- **1998-2013** **ITRS**: International Technology Roadmap for Semiconductors
  - Applied Moore’s Law to integrated circuits
  - Physical scaling worked until about 2004, then cores, 3D, ...
  - 2010: First selection of post-CMOS devices
- **2014-2015** **ITRS 2.0**
  - Driver changed from scaling to applications
  - 2015: Post-CMOS map of devices
- **2016+** **IRDS**: International Roadmap for Devices and Systems
  - Opened the door to non-semiconductor technologies
  - 2017: First roadmaps under development

Paolo Gargini
IRD Chair

Figure 1. Illustration of cross-team interactions for Beyond CMOS (BC).
IRDS BC Chapter Organization

Beyond CMOS

- **Emerging memory and storage devices**
  - Memory devices
  - Selector devices
  - Storage class memory devices
  - Person-in-charge: Matt Marinella

- **Emerging logic and information processing devices**
  - CMOS extension
  - Beyond-CMOS charge-based
  - Beyond-CMOS non-charge-based
  - Person-in-charge: Shamik Das

- **Emerging application areas**
  - Cryogenic electronics
  - Person-in-charge: Scott Holmes, Erik DeBenedictis

- **Emerging device and architecture interface**
  - Map Emerging architecture to suitable devices
  - Define FOMs and key challenges
  - Person-in-charge: Mike Frank, Paul Franzon, Matt Marinella, Geoff Burr

- **Assessment**
  - Define criteria
  - Based on the quantitative benchmarking reported by NRI
  - Person-in-charge: An Chen
Energy–Delay Metrics: Wiring

- **RQL**: Reciprocal Quantum Logic, a superconducting single flux quantum (SFQ) logic, $J_c = 100 \mu A/\mu m^2$
  - **JTL**: Josephson transmission line (0.13 fJ/bit, 5.5 ps)
  - **PTL**: passive transmission line (0.26 fJ/bit, 0.01–20 mm, 6.5 ps)

- 4.2 K operation; energy per bit at room temperature with 1000 W/W refrigeration (range $I_e$: 400–10,000 W/W)

- Source for RQL data:

- Added to:

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**Fig. 5.** Comparison between CMOS and spintronic devices in terms of (a) wire energy versus delay.
Can superconducting computing compete?
A better way to view the relationship

CMOS

SFQ
Lessons from an Emerging Technology

- Fair **metrics** are needed to evaluate alternative computing technologies
  - level the playing field to allow different technologies to compete
  - relevant lessons from hiring for diversity?

- Ramping up requires time **and resources**
  - the real Moore’s Law

- Government funding alone is not sufficient
  - cost to develop energy-efficient, large-scale computers is large
  - ramp up using smaller products and markets

- Don’t go it alone
  - use your mother elephant

- Go big or go home!
  - small improvements are not worth the effort
  - large disruptions require even larger advantages
References


  Video online: https://www.youtube.com/watch?v=3Whh9VXHqOQ


- International Roadmap for Devices and Systems (IRDS), http://irds.ieee.org/
Superconducting Computing in Large-Scale Hybrid Systems

D. Scott Holmes, Booz Allen Hamilton
Alan M. Kadin, Senior Member of IEEE
Mark W. Johnson, D-Wave Systems

Once focused solely on computation speed, superconducting computing is now proving useful in hybrid systems where its unique capabilities complement conventional computing technologies. Energy efficiency has become a strong motivation for developing large-scale superconducting systems.

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