Superconducting Computing at IARPA

Marc Manheimer
Program Manager
November 30, 2017
The Problem is Power-Space-Cooling

- Upgrading a facility to more powerful computers is constrained by
  - *Power* supply capability of electric company
  - *Space* limitations
  - *Cooling* infrastructure

- Constraints on developing computers with additional processing power
  - Some estimates to reach exascale are in the hundreds of megawatts.
  - An exascale computer at 20 megawatts based on semiconducting technology will require heroic measures.
  - We will require a different technology to get beyond exascale.

*A computer based on superconducting logic and cryogenic memory can help solve these issues*
Superconducting computing looks promising

Power (megawatts) vs. Performance (petaFLOPs per second)

- DOE Exascale Goal
- Top Computers
- Coral (USA) Goal, 2017
- Superconducting Goal

System Comparison (~20 PFLOP/s)

<table>
<thead>
<tr>
<th></th>
<th>Titan at ORNL</th>
<th>Superconducting Supercomputer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Performance</strong></td>
<td>17.6 PFLOP/s (#4 in world*)</td>
<td>20 PFLOP/s</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>710 TB (0.04 B/FLOPS)</td>
<td>5 PB (0.25 B/FLOPS)</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>8,200 kW avg. (not included: cooling, storage memory)</td>
<td>80 kW total power (includes cooling)</td>
</tr>
<tr>
<td><strong>Space</strong></td>
<td>4,350 ft² (404 m², not including cooling)</td>
<td>~200 ft² (includes cooling)</td>
</tr>
<tr>
<td><strong>Cooling</strong></td>
<td>additional power, space and infrastructure required</td>
<td>All cooling shown</td>
</tr>
</tbody>
</table>

* #1 in TOP500, 2012-11 (17.6 PFLOP/s)
Key Factors

• Approach based on:
  • Near-zero energy superconducting interconnect
  • New SFQ logic with no static power dissipation
  • New energy efficient cryogenic memory ideas
  • Optical ingress/egress
  • Commercial cryogenic refrigerators
C3 Goal:

Develop technologies for a computer based on superconducting logic with cryogenic memory, and

Integrate a prototype that can answer these questions:

1) Can we build a superconducting computer that is capable of solving important problems?

2) Does it provide a sufficient advantage over conventional computing that we want to build it?
Year Four Deliverables

- Logic: A 16-bit CPU that runs benchmark programs
- Memory: Small memory arrays controlled by SFQ circuitry
Program Addenda

- **SuperTools**
  - Develop design software tool chain for superconducting circuits
  - Kick-off was early November
  - Performers are Synopsys and USC

- **SuperCables**
  - Develop technology for energy efficient high speed interconnect between 4 kelvins digital circuits and room temperature
  - Proposers’ Day was early November
  - Aiming for awards in July
Cryogenic Egress: How is it done at present?

• Systems that require cryogenic information transfer
  • Naval RF receiver prototypes (an existing system with digital I/O)
  • Quantum computing
  • NASA radio astronomy,
  • NIST noise thermometry
  • Cryogenic Computing

• Electrical wires carry the signal
  • Coaxial cable
  • Twisted pairs
  • Cu/BeCu ribbon cable
Limitations of present approaches

- Poor scalability to high data transfer rates
  - Data rate per wire is small: 14 Gb/s per wire; ONR-Hypres
  - Thermal conductance of many-wire solution is too large
    - Example: One millimeter diameter, one meter long, Cu wire between 4 K and RT carries about 200 mW heat to 4 K. Compare with about 0.2 mW for glass fiber.
  - Problems increase with number of wires

- Unacceptable energy cost per bit
  - Above example leads to ~20 pJ/bit, just for heat leak, orders of magnitude above objective.
Today’s egress datalinks in receiver prototypes

- Electrical Datalink Chain
  - Drivers on superconductor IC
  - Transmission line from 4 to 300 K
  - Interface Amplifier
  - FPGA data receivers
What is new about your approach?

- Integrated optical-electrical system for high rate data transfer between 4 kelvins and room temperature
- New or improved features
  - Optical fiber to cryogenic space
  - Cryogenic electrical-to-optical modulators (EOM)
  - Pulse sequence generator (SFQ to EOM)
  - Superconducting ribbon cable
  - Optimized cryogenic amplifiers
  - High efficiency, cryogenic, optical-to-electrical modulators (OEM)
  - Data link error detection and correction
  - Advanced modulation schemes
One Notion of Cryogenic Photonic Data Flow

INPUT
- Laser
- Amplify and EOM
- Prep format for transport to 4 K
- Prep format for entry into COTS 300 K processor & ensure data integrity

300 K

Prep format for transport to 4 K
Amplify and EOM
Laser

Fiber to 4 K
OEM

Prep format for transport to 300 K
Amplify
EOM

Process
Receive at 4 K & prep for use (de-skew and buffer)
Coupling

4 K

Fiber to 300 K
Modulation enhancement
OEM
Why do you think that you can succeed?

• Industry is progressing towards integrated chip-level electro-optics

• Ideas for cryogenic electro-optic modulators surfaced by RFI

• New developments in data encoding enable optical fibers to carry data at ever increasing rates and at lower energy
If you succeed, what difference will it make?

High rate data transfer is an enabler for cryogenic applications of all of the following:

- Quantum computing
- Classical computing
- Digital radio
- Streaming data processing
**SuperCables** Program Organization

- This program: Technology development (24 months):
  Set of themed projects to develop and evaluate technology for data transmission
  - Cryogenic electrical-to-optical modulators (EOM)
  - Programmable SFQ generator system (stimulus module)
  - Test and evaluation system

- Next program: Maturation and integration (36 months):
  Integrators mature technologies and integrate system
  - Cryogenic optical-to-electrical modulator (OEM)
  - Test and evaluation team measures system performance
  - System model will predict scaling behavior and opportunities
SuperCables Proposed Work

- Test probe and system specification and design (T&E)
  - Energy measurement capable
  - Bit error rate measurement capable
  - Allow for various electrical-to-optical modulators (EOM)
- Pulse sequence generator (T&E)
  - Based on single flux quanta
  - Chip fabricated by Lincoln Laboratory
  - Able to generate pseudorandom pulse sequence
  - Able to supply pulses for any EOM in program
- Cryogenic electro-optic modulators (performers)
- Other?
How hard is this problem?

- Very Hard!
  - Developing a cryogenic modulator that has sufficient bandwidth and energy efficiency
  - Developing a pulse generator that is sufficiently energy efficient
  - Developing sufficiently low loss interfaces between disparate transmission subsystems and components

- Where does our energy goal come from?
  - Energy per bit at 4 K = (2E6 W)(0.05)/(1E18/s*500) = 200 aJ

- Lower energy per bit will enable higher data rate streaming applications.
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<tr>
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<th>Unit</th>
<th>Exascale goal</th>
<th>Objective</th>
<th>Stretch</th>
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<tbody>
<tr>
<td>Energy</td>
<td>aJ</td>
<td>2 MW total</td>
<td>200</td>
<td>10</td>
</tr>
<tr>
<td>Data Egress</td>
<td>aJ</td>
<td>100</td>
<td>100</td>
<td>10</td>
</tr>
<tr>
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<td>ns</td>
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<td>Energy per bit at 4 K</td>
<td>aJ/bit</td>
<td>2,000</td>
<td>200</td>
<td>10</td>
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<tr>
<td>Channels per chip area</td>
<td>cm⁻²</td>
<td>10</td>
<td>20</td>
<td>100</td>
</tr>
<tr>
<td>Data rate per channel</td>
<td>Gbit/s</td>
<td>10</td>
<td>50</td>
<td>100</td>
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**SuperCables** Metrics and Goals

- Photonic ingress & egress components (Performers)
  - Bit energy at 4 K: 10 aJ/bit (this is about 50 flux quanta or about 100 photons)
  - Data rate: 100 Gb/s per channel

- Pulse sequence generator (Test and Evaluation team)
  - Input: 10 single flux quanta; Output: pulses up to 100 mV, 100 ps wide
  - 4 pulses proven by month 18

- Cryogenic test bed designed and built by month 12 (T&E)

- System (next program, notional)
  - Data rate: 640 Gb/s, ingress or egress
  - Bit error rate: $10^{-6}$ raw; $10^{-12}$ with more energy, more error correction, or slower rate
  - Modularity: New component can replace old with minimal redo of link, clear interface control documentation
### SuperCables Notional Pre-Launch Schedule

<table>
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<th>Activity</th>
<th>Date</th>
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<tbody>
<tr>
<td>Proposers Day</td>
<td>November 7</td>
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<tr>
<td>BAA Draft Feedback Due</td>
<td>November 17</td>
</tr>
<tr>
<td>BAA Release</td>
<td>January 8</td>
</tr>
<tr>
<td>Proposals Due</td>
<td>February 19</td>
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<tr>
<td>Award</td>
<td>July 30</td>
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